General Description

The SET4038 is an 8-channel, 32-bit DAC designed for digital audio systems. Its internal circuitry boasts a state-of-the-art 32-bit digital filter that optimizes both audio quality and short group delay. With support for a maximum 192kHz PCM input, it is ideal for reproducing high-resolution audio sources that are increasingly common in network audios, USB-DACs and car audio systems.

Furthermore, the SET4038 incorporates the innovative OSR-doubler technology, enabling it to handle a diverse range of signals while minimizing out-of-band noise and maintaining low power consumption. Additionally, the device provides three types of 32-bit digital filters, which can enable sound making simple and flexible in wide range of applications. It should be noted that SET4038 needs to input the MCLK signal in advance to execute the 3-wire serial/I2C-bus program.

The SET4038 is available in a Green TQFN-5×5-32FL package.

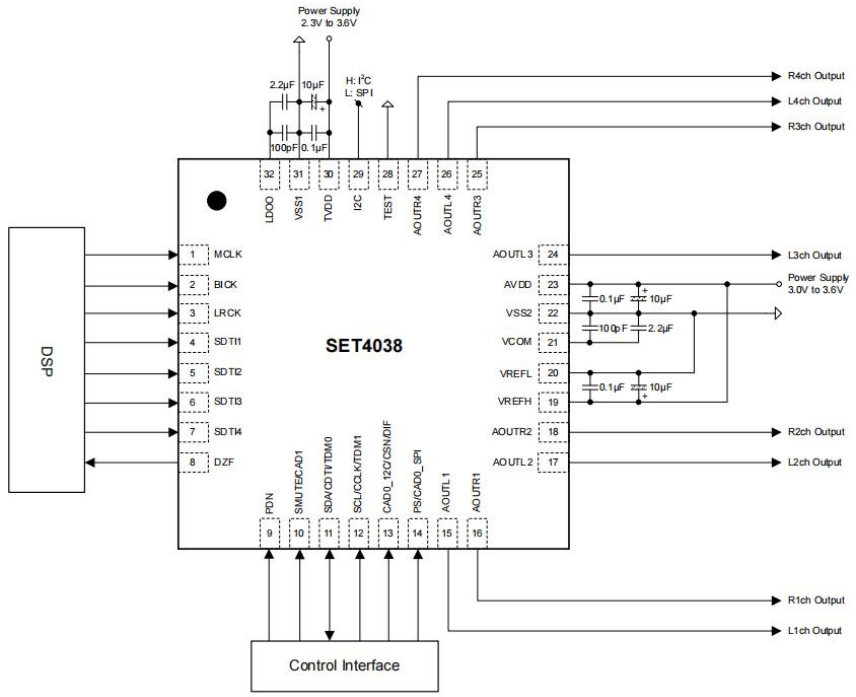
Features

- 8ch 32bit DAC
  - 256 x Over sampling
  - 32-bit High Quality Sound Short Delay Digital Filter
  - Single-ended Output, Smoothing Filter
  - THD+N: 91dB
  - DR, S/N: 110dB
  - Channel Independent Digital Volume Control (0dB ~ -127dB, 0.5dB Step, Mute)
  - Soft Mute
  - De-emphasis Filter (supporting 32kHz, 44.1kHz and 48kHz)
  - I/F Format: MSB justified, LSB justified, I2S, TDM
  - Zero Detection
- µP Interface: 3-wire Serial/ I2C bus(Fast Speed Mode: 400kHz) / Parallel Mode
- Power Supply
  - Analog Supply: AVDD = 3.0 ~ 3.6V
  - In/Output Buffer: TVDD =2.3~3.6V
  - Integrated LDO for Digital Power Supply
- Operating Temperature: Ta = - 40 ~ 105℃
- Package: TQFN-5×5-32FL(0.5mm pitch)

Applications

- External Amplifiers
- Car Audios System
- CD Players
- Headphones
- Professional Measuring Instruments
- USB DACs

Typical Application



NOTE: 1. The SET4038 includes smoothing filters.

Figure 1. Typical Application Circuit

Block Diagrams

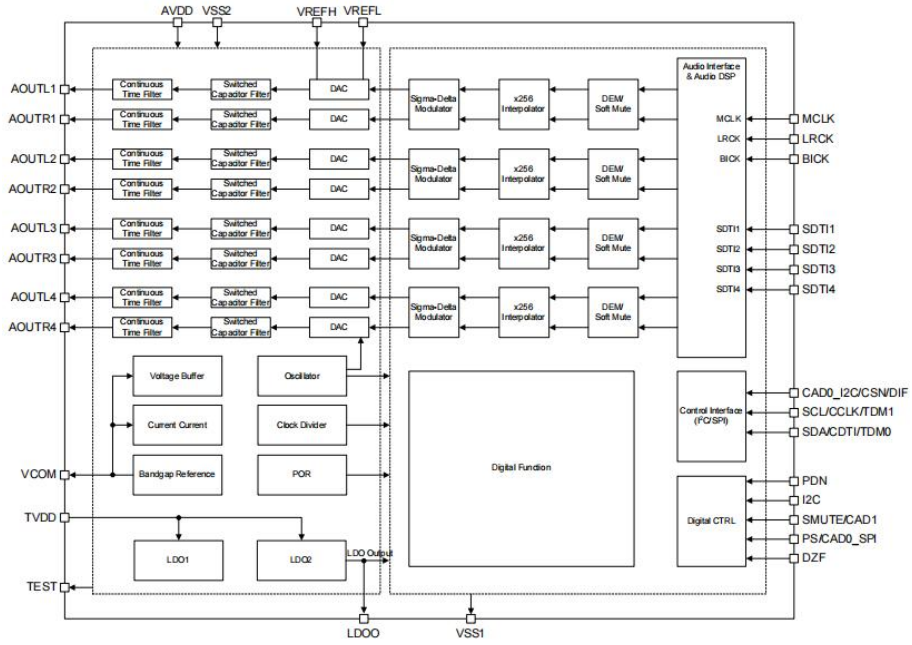
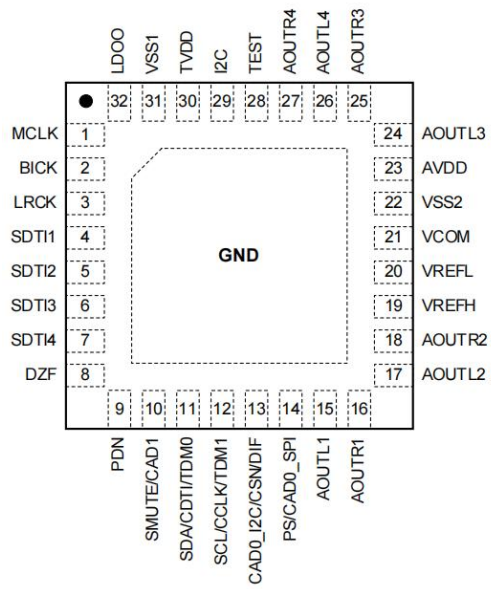


Figure 2. Block Diagram

Pin Configurations

(TOP VIEW)



TQFN-5×5-32FL

PIN DESCRIPTION

PIN	NAME	TYPE	POWER-DOWN STATE	FUNCTION
1	MCLK	I	Hi-Z	Master Clock Input Pin (External).
2	BICK	I	Hi-Z	Serial Audio Input Bit Clock Pin.
3	LRCK	I	Hi-Z	Serial Audio Input Left/Right Clock Pin.
4	SDTI1	I	Hi-Z	Serial Audio Input Data Port.
5	SDTI2	I	Hi-Z	Serial Audio Input Data Port.
6	SDTI3	I	Hi-Z	Serial Audio Input Data Port.
7	SDTI4	I	Hi-Z	Serial Audio Input Data Port.
8	DZF	O	50kΩ Pull-Down	Zero Detection Function Pin. When the input data of each channel reaches zero continuously within 8192 LRCK cycles, the DZF pin becomes high. When the input data of each channel does not reach zero, the DZF pin immediately reverts to the low level.
9	PDN	I	Hi-Z	Power-Down Pin. When it is low, the SET4038 enters a power-down mode, and its control registers revert to their default settings.
10	SMUTE	I	Hi-Z	Soft Mute Pin in Parallel Control Mode. When SMUTE pin becomes high, the soft mute cycle is activated. When returning low, the output mute is released.
	CAD1	I		Chip Address 1 Pin in the I2C-Bus or 3-Wire Serial Control Mode. It serves as an identifier for the specific chip or device being addressed.
11	SDA	I/O	Hi-Z	Control I/O Data Line in I2C-Bus Mode.
	CDTI	I		Output Data Pin. It is from the control port interface in 3-wire serial control mode.
	TDM0	I		Function Pin 0. It is used as the selector for the TDM mode in the parallel control mode.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	POWER-DOWN STATE	FUNCTION
12	SCL	I	Hi-Z	Serial Control Interface Clock Pin in I2C-Bus Serial Control Mode. It is used to clock control data bits into and out of the SET4038.
	CCLK	I		Serial Control Interface Clock in 3-Wire Serial Control Mode. It is used to clock control data bits into the SET4038.
	TDM1	I		Function Pin 1. It is used as the selector for the TDM mode in the parallel
13	CAD0_I2C	I	Hi-Z	Chip Address 0 Pin in the I^2C-Bus Mode. It serves as an identifier for the specific chip or device being addressed.
	CSN	I		Control Port Enable Pin in 3-Wire Serial Control Mode. It is used to enable the control port interface on the SET4038.
	DIF	I		Audio Data Format Select Pin in Parallel Control Mode. Low: 32-bit MSB. High: 32-bit I2S.
14	PS	I	Hi-Z	Control Mode Select Pin (I2C Pin = High). Low: I2C-bus serial control mode. High: parallel control mode.
	CAD0_SPI	I		Chip Address 0 Pin (I2C Pin = Low) in 3-Wire Serial Control Mode. It serves as an identifier for the specific chip or device being addressed.
15	AOUTL1	O	Hi-Z	Left Channel Analog Output Pin.
16	AOUTR1	O	Hi-Z	Right Channel Analog Output Pin.
17	AOUTL2	O	Hi-Z	Left Channel Analog Output Pin.
18	AOUTR2	O	Hi-Z	Right Channel Analog Output Pin.
19	VREFH	–	Hi-Z	High Voltage Reference Input Pin. It should be connected to the AVDD.
20	VREFL	–	Hi-Z	Low Voltage Reference Input Pin. It should be connected to the VSS2.
21	VCOM	O	500Ω Pull-Down	Common Voltage Output Pin (AVDD × 1/2). Use a large external capacitor around 2.2μF to reduce power noise.
22	VSS2	–	–	Analog Ground Pin. Ground for the analog circuitry in the chip.
23	AVDD	P	–	Analog Power Supply Pin. The voltage range is from 3.0V to 3.6V.
24	AOUTL3	O	Hi-Z	Left Channel Analog Output Pin.
25	AOUTR3	O	Hi-Z	Right Channel Analog Output Pin.
26	AOUTL4	O	Hi-Z	Left Channel Analog Output Pin.
27	AOUTR4	O	Hi-Z	Right Channel Analog Output Pin.
28	TEST	–	21.5kΩ Pull-Down	TEST pin. It should be connected to VSS1.
29	I2C	I	Hi-Z	Control Mode Select Pin. Low: 3-wire serial control mode. High: I2C-bus serial control mode or parallel control mode.
30	TVDD	P	–	Digital Power Supply Pin. The voltage range is from 2.3V to 3.6V.
31	VSS1	–	–	Digital Ground Pin.
32	LDOO	O	630Ω Pull-Down	LDO Output Pin. The pin requires a connection to ground via a 2.2uF capacitor with a tolerance of ±50%.
Exposed Pad	GND	–	–	The exposed pad on the bottom surface of the package should be connected to the ground plane for optimized heat dissipation.

NOTES:

1. I = input, O = output, I/O = input or output, P=power.
2. All digital inputs must be securely connected and not allowed to remain unconnected or floating

Electrical Characteristics

(AVDD = TVDD = VREFH = 3.3V, VSS1 = VSS2 = 0V, T_A = +25°C , unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC Analog Output							
Resolution					32		Bits
Output Voltage (2)					2.8		Vpp
Total Harmonic Distortion +Noise (0dBFS)	THD + N	f_S = 48kHz (3)			91		dB
		f_S = 96kHz (3)			90		
		f_S = 192kHz			86		
Dynamic Range (-60dBFS)	DR	f_S = 48kHz (A-weighted)			110		dB
		f_S = 96kHz			103		
		f_S = 192kHz			102		
Signal to Noise Ratio	SNR	f_S = 48kHz (A-weighted)			110		dB
		f_S = 96kHz			103		
		f_S = 192kHz			103		
Interchannel Isolation		Isolation from other LR channels			109		dB
		Isolation of LR for a single channel			105		
Interchannel Gain Mismatch					0		dB
Load Resistance (4)	R_L				5/10		kΩ
Load Capacitance	C_L				40		pF
Power Supply Rejection	PSR	AVDD(5)			65		dB
		TVDD(6)			88		
		VREFH(7)			82		
Power Supply							
Power Supply Current	I_{AVDD}	Normal operation(PDN pin = high)	f_S = 48kHz, 96kHz, 192kHz		14		mA
	I_{TVDD}		f_S = 48kHz		14		
			f_S = 96kHz		25		
			f_S = 192kHz		35		
	I_{VREFH}		f_S = 48kHz, 96kHz, 192kHz		2.5		
Power Supply Leakage Current	I_{AVDD} + I_{TVDD} + I_{VREFH}	Power-down mode (PDN pin = low) (8)			80		nA

NOTES:

1. Measurement frequency f_s = 48kHz, BICK = 64 × f_S, signal frequency = 1kHz, 32-bit data, 20Hz to 20kHz at f_s = 48kHz, 20Hz to 40kHz at f_s = 96kHz, 20Hz to 40kHz at f_s = 192kHz.
2. Full-scale output voltage is always proportional to AVDD. Specifically, it is calculated as AVDD multiplied by 0.86.
3. Test conditions 48kHz/96kHz are done in high-performance mode for optimized performance.
4. AC load = 5kΩ , DC load = 10kΩ .
5. The PSRR is measured by applying a 1kHz sine wave with a peak-to-peak amplitude of 50mV to the AVDD.
6. The PSRR is measured by applying a 1kHz sine wave with a peak-to-peak amplitude of 50mV to the TVDD.
7. The PSRR is measured by applying a 1kHz sine wave with a peak-to-peak amplitude of 50mV to the VREFH.
8. Quiescent current is measured when all digital input pins, inclusive of clock pins, are connected to VSS.

Electrical Characteristics

(AVDD = TVDD = VREFH = 3.3V, VSS1 = VSS2 = 0V, T_A= +25°C , unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
High-Level Input Voltage	V_{IH}				1.8		V
Low-Level Input Voltage	V_{IL}				1.3		V
High-Level Output Voltage	V_{OH}	DZF pin, I_{OUT} = -100µA			3.29		V
Low-Level Output Voltage	V_{OL}	DZF pin, $_{IOUT}$ = 100µA			0.01		V
Input Leakage Current	I_{IN}				1		µA
Digital Filter Characteristics with Sharp Roll-Off Filter (2)							
Pass Band (3)	PB	f_S = 48kHz	±0.05dB		0 ~ 22		kHz
			-3.0dB		23.5		
Pass Band Ripple (4)	PR				±0.003		dB
Stop Band (3)	SB				26.4		kHz
Stop Band Attenuation (6)	SA				80		dB
Group Delay (5)	GD				26.8		1/fS
Frequency Response (Digital filter + SCF + SMF (6))			0 to 20kHz		-0.03 ~ 0.12		dB
Pass Band (3)	PB	f_S = 96kHz	±0.05dB		0 ~ 44		kHz
			-3.0dB		47		
(4) Pass Band Ripple	PR				±0.003		dB
Stop Band (3)	SB				52.8		kHz
Stop Band Attenuation (6)	SA				80		dB
Group Delay (5)	GD				26.8		$1/f_S$
Frequency Response (Digital filter + SCF + SMF (6))			0 to 20kHz		-0.03 ~ 0.12		dB
Pass Band (3)	PB	f_S = 192kHz	±0.05dB		0 ~ 88		kHz
			-3.0dB		94		
(4) Pass Band Ripple	PR				±0.003		dB
Stop Band (3)	SB				105.6		kHz
Stop Band Attenuation (6)	SA				80		dB
Group Delay (5)	GD				26.8		$1/f_S$
Frequency Response (Digital filter + SCF + SMF (6))			0 to 20kHz		-0.03 ~ 0.1		dB

NOTES:

1. Measurement frequency f_S = 48kHz, BICK = 64 × f_S, signal frequency = 1kHz, 32-bit data, 20Hz to 20kHz at f_S = 48kHz, 20Hz to 40kHz at f_S = 96kHz, 20Hz to 40kHz at f_S = 192kHz.
2. Specified by design and characterization, not production tested.
3. The frequencies of the pass band and stop band are scalable based on the sampling frequency f_S. For instance, PB = 0.45 × f_S, SB = 0.55 × f_S.
4. The pass band gain amplitude of the double oversampling filter is exhibited during the initial stage of the interpolator operation.
5. The delay time that arises from digital filtering is the duration from the moment when 16/20/24/32-bit data for both channels is set in the input register to the point when the analog signal is outputted.
6. When a 1kHz sine wave with 0dB is inputted, the output level is presumed to be 0dB.

Electrical Characteristics

(AVDD = TVDD = VREFH = 3.3V, VSS1 = VSS2 = 0V, T_A = +25°C , unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Filter Characteristics with Slow Roll-Off Filter (2)							
Pass Band (3)	PB	f_S= 48kHz	±0.05dB		0 ~ 14.58		kHz
			-3.0dB		21.74		
(4) Pass Band Ripple	PR				±0.003		dB
Stop Band (3)	SB				36		kHz
Stop Band Attenuation (6)	SA				88.66		dB
Group Delay (5)	GD				6.85		1/fS
Frequency Response (Digital filter + SCF + SMF (6))			0 to 20kHz		-3.2 ~ 0		dB
Pass Band (3)	PB	f_S= 96kHz	±0.05dB		0 ~ 29.16		kHz
			-3.0dB		43.48		
(4) Pass Band Ripple	PR				±0.003		dB
Stop Band (3)	SB				72		kHz
Stop Band Attenuation (6)	SA				88.66		dB
Group Delay (5)	GD				6.85		1/fS
Frequency Response (Digital filter + SCF + SMF (6))			0 to 20kHz		-3.2 ~ 0		dB
Pass Band (3)	PB	f_S= 192kHz	±0.05dB		0 ~ 58.32		kHz
			-3.0dB		86.96		
(4) Pass Band Ripple	PR				±0.003		dB
Stop Band (3)	SB				144		kHz
Stop Band Attenuation (6)	SA				88.66		dB
Group Delay (5)	GD				6.85		1/f_S
Frequency Response (Digital filter + SCF + SMF (6))			0 to 20kHz		-0.03 ~ 0		dB

NOTES:

1. Measurement frequency f_S = 48kHz, BICK = 64 × f_S, signal frequency = 1kHz, 32-bit data, 20Hz to 20kHz at f_S = 48kHz, 20Hz to 40kHz at f_S = 96kHz, 20Hz to 40kHz at f_S = 192kHz.
2. Specified by design and characterization, not production tested.
3. The frequencies of the pass band and stop band are scalable based on the sampling frequency f_S. For instance, PB = 0.25 × f_S, SB = 0.75 × f_S.
4. The pass band gain amplitude of the double oversampling filter is exhibited during the initial stage of the interpolator operation.
5. The delay time that arises from digital filtering is the duration from the moment when 16/20/24/32-bit data for both channels is set in the input register to the point when the analog signal is outputted.
6. When a 1kHz sine wave with 0dB is inputted, the output level is presumed to be 0dB.

Timing Characteristics

(AVDD = TVDD = VREFH = 3.3V, VSS1 = VSS2 = 0V, T_A = +25°C , unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Master Clock Timing							
External Clock	Frequency	f_{CLK}	128 × f_{SN}, 128 × f_{SD}, 192 × f_{SN}, 256 × f_{SN}		1.024 ~ 12.288		MHz
	Pulse Width Low	t_{CLKL}			29.6		ns
	Pulse Width High	t_{CLKH}			29.6		ns
	Frequency	f_{CLK}	192 × f_{SD}, 384 × f_{SN}		3.072 ~ 18.432		MHz
	Pulse Width Low	t_{CLKL}			21.6		ns
	Pulse Width High	t_{CLKH}			21.2		ns
	Frequency	f_{CLK}	512 × f_{SN}, 256 × f_{SD}, 128 × f_{SQ}		4.096 ~ 24.576		MHz
	Pulse Width Low	t_{CLKL}			15.2		ns
	Pulse Width High	t_{CLKH}			13.2		ns
LRCK Timing (Slave Mode)							
LRCK Frequency	Normal Speed Mode	f_{SN}	Normal mode (TDM1-0 bits = 00)		8 ~ 48		kHz
	Double Speed Mode	f_{SD}			48 ~ 96		kHz
	Quad Speed Mode	f_{SQ}			96 ~ 192		kHz
Duty Cycle		D_{uty}			50		%
LRCK Frequency	Normal Speed Mode	f_{SN}	TDM128 mode (TDM1-0 bits = 01)		8 ~ 48		kHz
	Double Speed Mode	f_{SD}			48 ~ 96		kHz
	Quad Speed Mode	f_{SQ}			96 ~ 192		kHz
High Time		t_{LRH}			35.2		ns
Low Time		t_{LRL}			35.2		ns
LRCK Frequency	Normal Speed Mode	f_{SN}	TDM256 mode (TDM1-0 bits = 10)		8 ~ 48		kHz
	Double Speed Mode	f_{SD}			48 ~ 96		kHz
High Time		t_{LRH}			35.2		ns
Low Time		t_{LRL}			35.2		ns
LRCK Frequency	Normal Speed Mode	f_{SN}	TDM512 mode (TDM1-0 bits = 11)		8 ~ 48		kHz
High Time		t_{LRH}			35.2		ns
Low Time		t_{LRL}			35.2		ns

Timing CHharacteristics

(AVDD = TVDD = VREFH = 3.3V, VSS1 = VSS2 = 0V, T_A = +25°C , unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Audio Interface Timing							
BICK Period	Normal Speed Mode	t_{BCK}	Normal mode (TDM1-0 bits = 00)		81.6		ns
	Double Speed Mode				82		ns
	Quad Speed Mode				81.6		ns
BICK Pulse Width Low		t_{BCKL}			14		ns
BICK Pulse Width High		t_{BCKH}			14.8		ns
LRCK Edge to BICK ↑ (1)		tLRB			5		ns
BICK ↑ to LRCK Edge (1)		t_{BLR}			5		ns
SDTI Hold Time		t_{SDH}			5		ns
SDTI Setup Time		t_{SDS}			4.8		ns
BICK Period	Normal Speed Mode	t_{BCK}	TDM128 mode (TDM1-0 bits = 01)		163.2		ns
	Double Speed Mode				81.6		ns
	Quad Speed Mode				41.2		ns
BICK Pulse Width Low		t_{BCKL}			14.4		ns
BICK Pulse Width High		t_{BCKH}			14.6		ns
LRCK Edge to BICK ↑ (1)		t_{BLR}			4.6		ns
BICK ↑ to LRCK Edge (1)		t_{LRB}			4.8		ns
SDTI Hold Time		t_{SDH}			4.8		ns
SDTI Setup Time		t_{SDS}			4.2		ns
BICK Period	Normal Speed Mode	t_{BCK}	TDM256 mode (TDM1-0 bits = 10)		81.6		ns
	Double Speed Mode				40.8		ns
BICK Pulse Width Low		t_{BCKL}			14.4		ns
BICK Pulse Width High		t_{BCKH}			15.6		ns
LRCK Edge to BICK ↑ (1)		t_{BLR}			4.6		ns
BICK ↑ to LRCK Edge (1)		t_{LRB}			5		ns
SDTI Hold Time		t_{SDH}			5		ns
SDTI Setup Time		t_{SDS}			5		ns
BICK Period	Normal Speed Mode	t_{BCK}	TDM512 mode (TDM1-0 bits = 11)		40.8		ns
BICK Pulse Width Low		t_{BCKL}			14.8		ns
BICK Pulse Width High		t_{BCKH}			14.8		ns
LRCK Edge to BICK ↑ (1)		t_{BLR}			4.8		ns
BICK ↑ to LRCK Edge (1)		t_{LRB}			5		ns
SDTI Hold Time		t_{SDH}			5		ns
SDTI Setup Time		t_{SDS}			4.6		ns

NOTE:

1. The occurrence of the BICK rising edge does not overlap with the LRCK edge, ensuring proper synchronization and avoiding potential conflicts.

Timing Characteristics

(AVDD = TVDD = VREFH = 3.3V, VSS1 = VSS2 = 0V, T_A = +25°C , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Control Interface Timing (3-Wire Serial Mode)						
CCLK Period	t_{CCK}			190		ns
CCLK Pulse Width Low	t_{CCKL}			66.4		ns
CCLK Pulse Width High	t_{CCKH}			68		ns
CDTI Setup Time	t_{CDS}			20.8		ns
CDTI Hold Time	t_{CDH}			21.6		ns
CSN High Time	t_{CSW}			128		ns
CSN ↑ to CCLK ↑	t_{CSS}			10.4		ns
CCLK ↑ to CSN ↑	t_{CSH}			36.8		ns
Control Interface Timing (I^2C-Bus Mode)						
SCL Clock Frequency	f_{SCL}			400		kHz
Bus Free Time between Transmissions	t_{BUF}			0.4		µs
Start Condition Hold Time	t_{HD_STA}	Prior to first clock pulse		0.165		µs
Clock Low Time	t_{LOW}			0.78		µs
Clock High Time	t_{HIGH}			0.41		µs
Setup Time for Repeated Start Condition	t_{SU_STA}			0.1		µs
SDA Hold Time from SCL Falling (1)	t_{HD_DAT}			0		µs
SDA Setup Time from SCL Rising	t_{SU_DAT}			0.1		µs
Rise Time of Both SDA and SCL Lines	t_R			1		µs
Fall Time of Both SDA and SCL Lines	t_F			0.3		µs
Setup Time for Stop Condition	t_{SU_STO}			0.15		µs
Pulse Width of Spike Noise Suppressed by Input Filter	t_{SP}			50		ns
Capacitive Load on Bus	C_B			400		pF
Power-Down/Reset Timing						
PDN Pulse Width (2)	t_{APD}			600		ns
PDN Reject Pulse Width	t_{RPD}			50		ns

NOTES:

1. The data must be maintained for an adequate duration to span the 300ns transition period of SCL, ensuring stable and accurate transmission.

2. To reset the SET4038, the PDN pin is recommended to be low during power-up, and this low state must be maintained for a duration exceeding 600ns to ensure a complete reset. Conversely, a low pulse lasting less than 50ns will not trigger a reset in the SET4038.

Timing Diagram

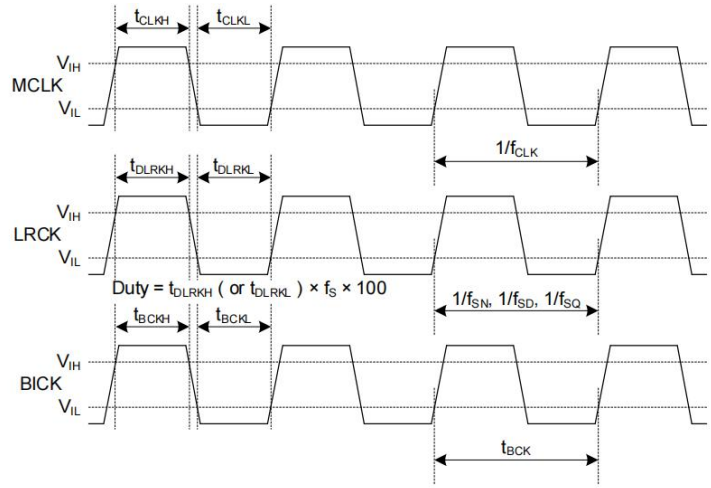


Figure 1. Non-TDM Clock Timing

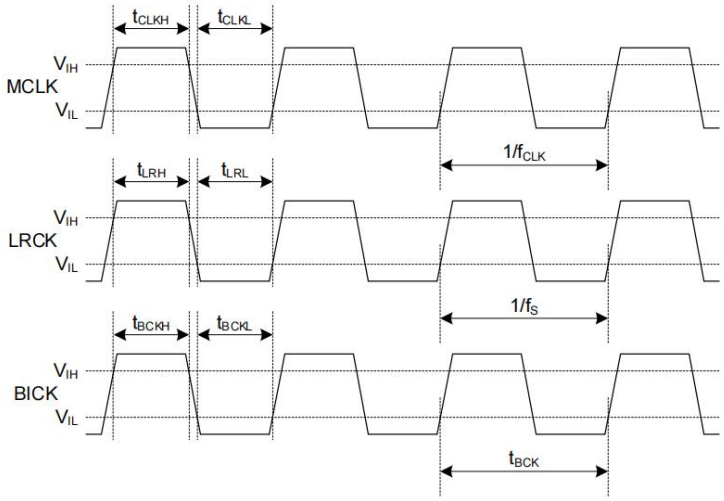


Figure 2. TDM Clock Timing

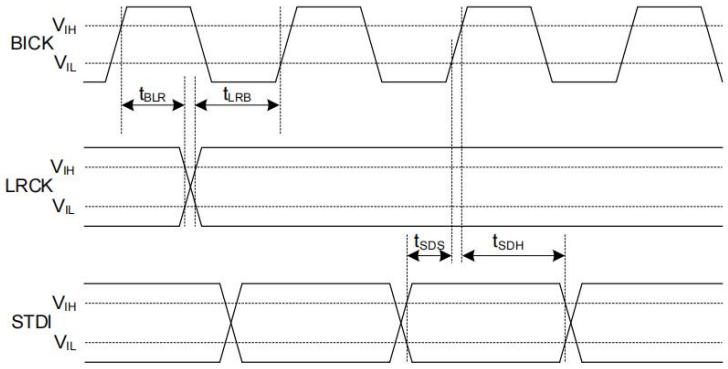


Figure 3. Non-TDM Clock Timing (Audio Interface)

Timing Diagram(continued)

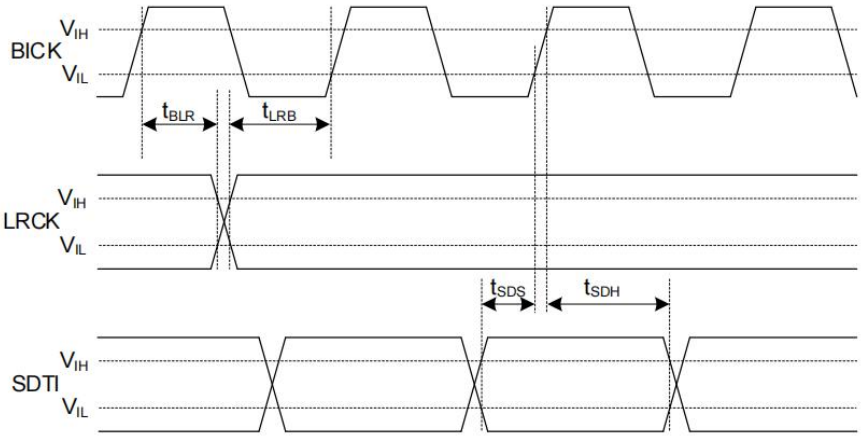


Figure 4. TDM Clock Timing (Audio Interface)

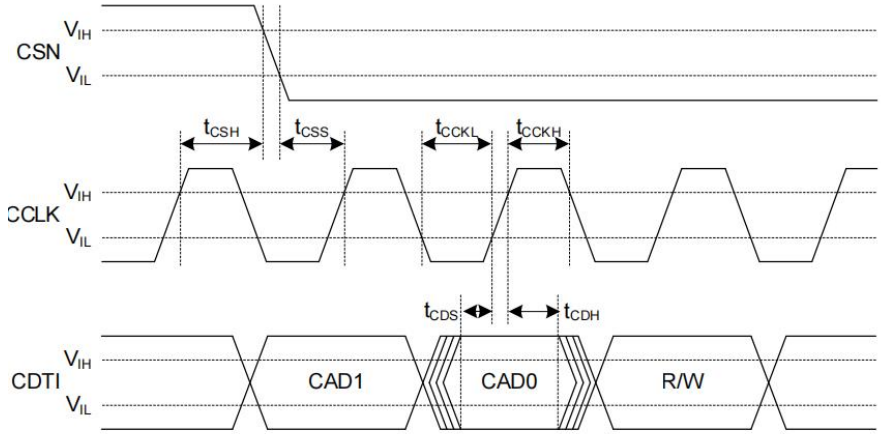


Figure 5. 3-Wire Serial Mode Command Input Timing (Write Only)

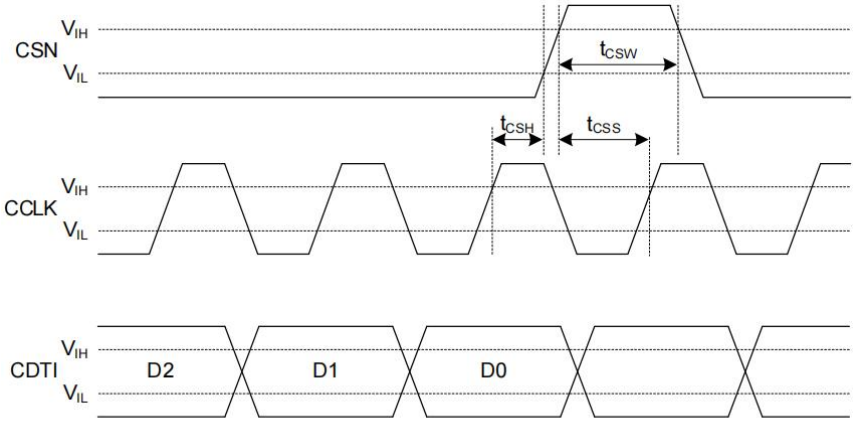


Figure 6. 3-Wire Serial Mode Data Input Timing (Write Only)

Timing Diagram(continued)

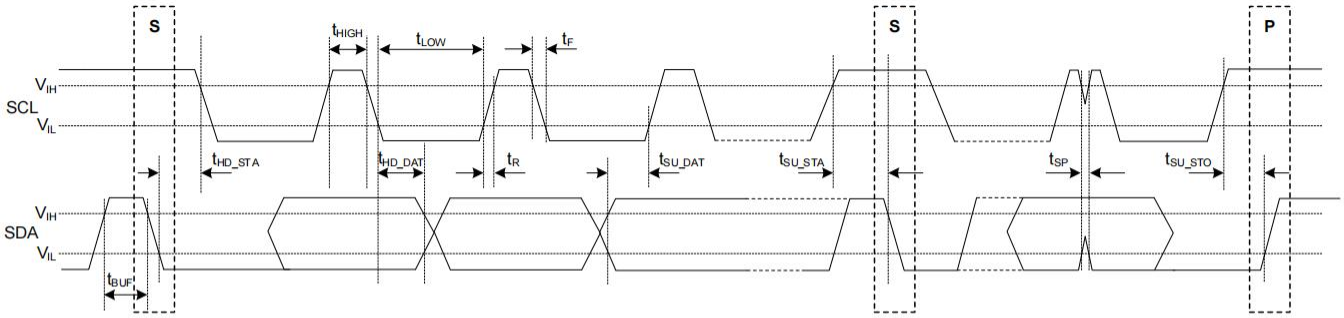


Figure 7. I²C-Bus Mode Input/Output Timing (Write/Read)

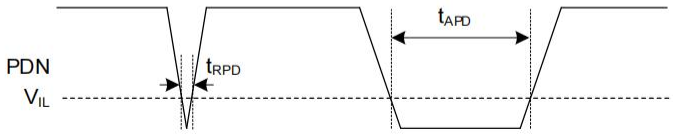
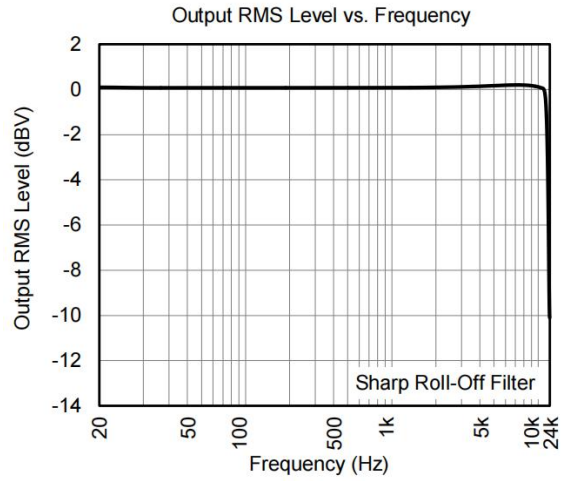
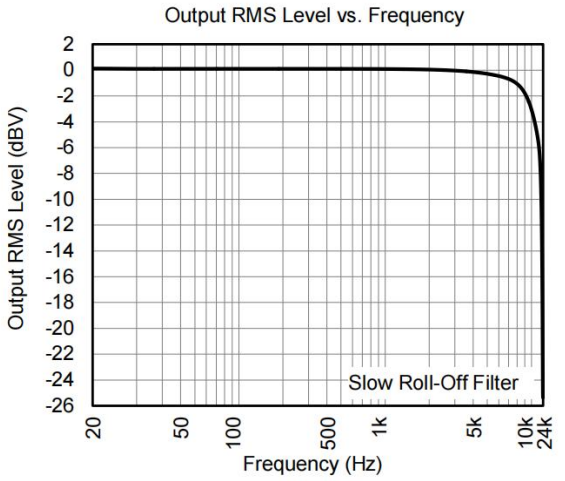


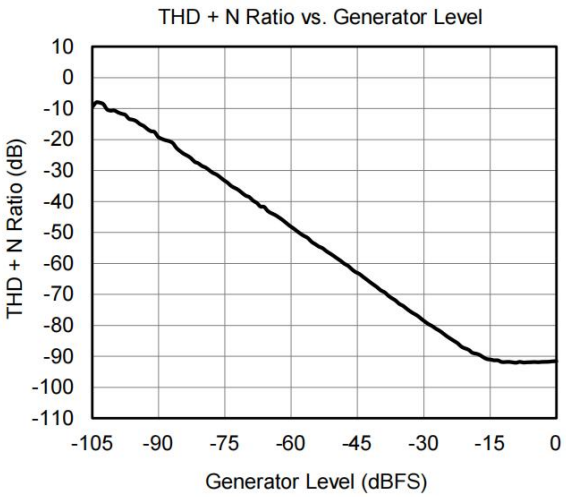
Figure 8. Power-Down/Reset Timing

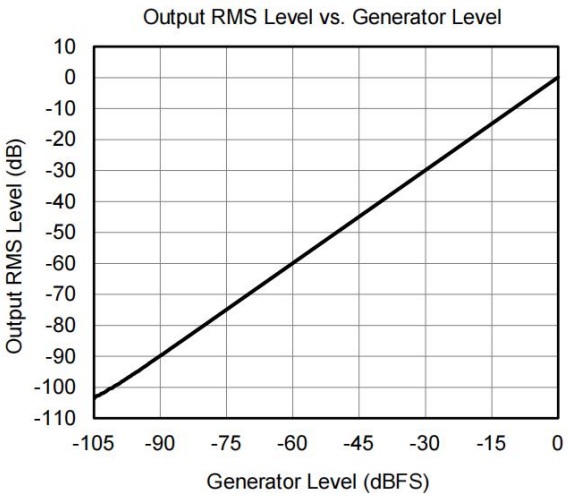
TYPICAL PERFORMANCE CHARACTERISTICS

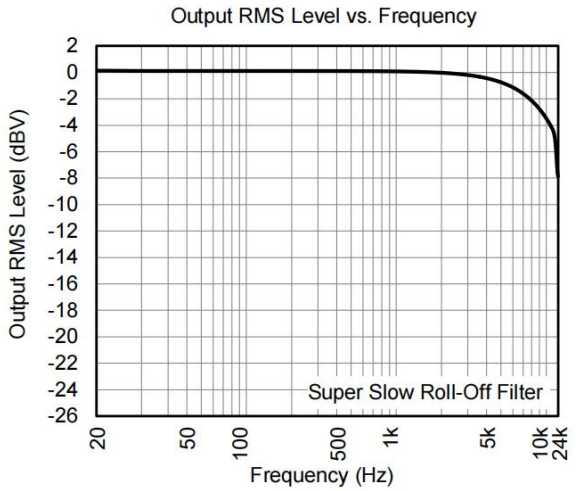
T_A = +25°C , AVDD = TVDD = VREFH = 3.3V, VSS1 = VSS2 = 0V. Measurement frequency f_S = 48kHz, BICK = 64 × f_S =3.072MHz, MCLK = 12.288MHz, signal frequency = 1kHz, 20Hz to 20kHz at 48kHz, 32-bit data, DFS2-0 bits = 001, I^2S mode.

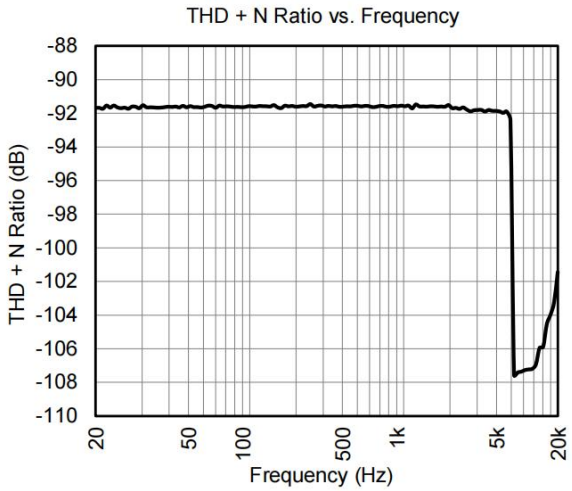




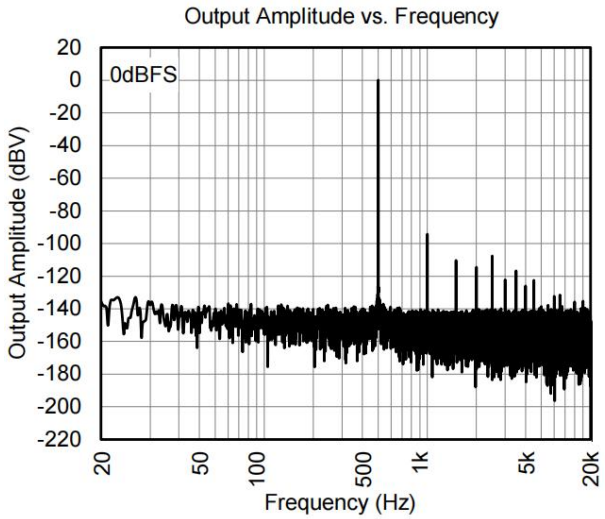


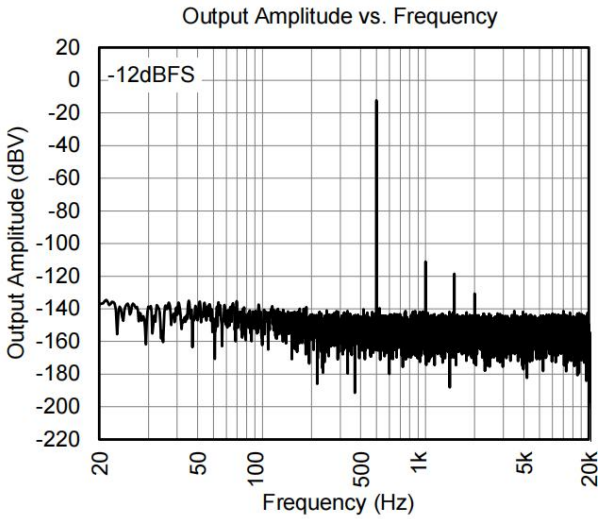


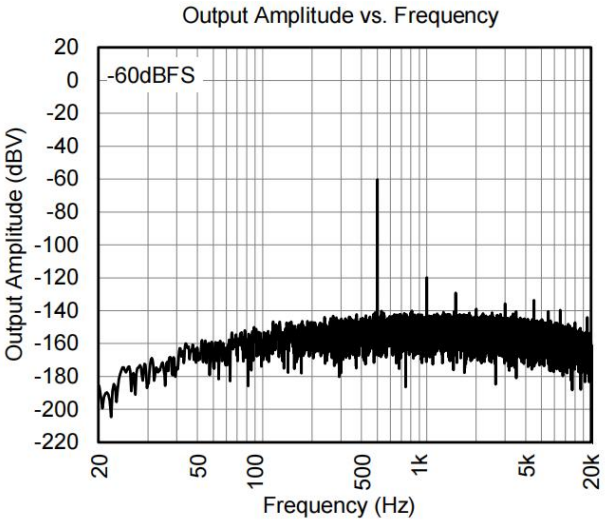


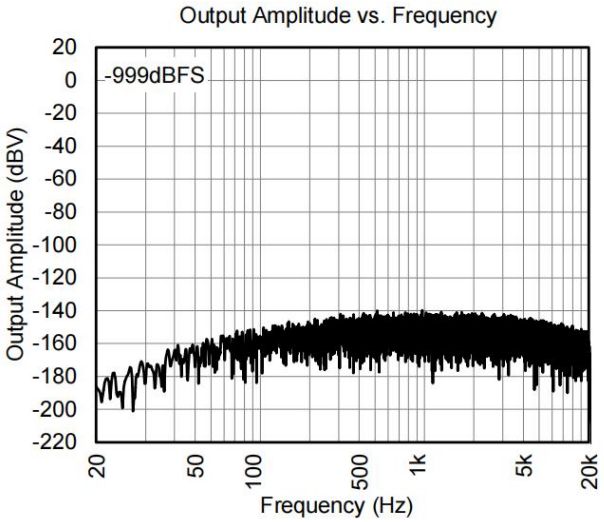


Typical Characteristics









DETAILED DESCRIPTION

System Clock

The SET4038 requires three external clocks (MCLK, LRCK and BICK) for its operation. These clocks are crucial for ensuring the proper synchronization and transmission of data within the device. MCLK should be synchronized with LRCK and BICK, even if this stage is not the most important. The DFS2-0 bits in Table 1 are responsible for determining the sampling speed. At each specific sampling speed, the frequency of MCLK is automatically configured according toTable 2, ensuring seamless and accurate data transmission.

When the reset is exited during power-up (PDN pin = low-to-high state), the SET4038 remains in power-down mode until both MCLK and LRCK signals are entered The SET4038 is configured to operate in manual mode upon power-up, with the PDN pin transitioning from a low-to-high state. When it comes to adjusting the clock settings, it is crucial to reset the SET4038 either by manipulating the PDN pin or by utilizing the RSTN bit. This reset ensures that the device can accommodate the new clock configurations and operate reliably.

In case that the clock is paused, a click noise will emit when it is restarted. If the click noise poses an issue for system applications, it is recommended to externally mute the digital output.

Manual Setting Mode

The SET4038 automatically detects the frequency of the MCLK, and the DFS2-0 bits in Table 1 are responsible for configuring the sampling rate. It is crucial to provide the appropriate MCLK frequency externally for each sampling speed, as specified in Table 2, to ensure accurate and reliable data transmission. The SET4038 is configured to operate in manual mode upon power-up, with the PDN pin transitioning from a low-to-high state. When the DFS2-0 bits undergo changes, it is necessary to reset the SET4038 through the RSTN bit.

Table 1. Sampling Speed in Manual Setting Mode

DFS2 Bit	DFS1 Bit	DFS0 Bit	Sampling Speed Mode (fS)	
0	0	0	Normal Speed Mode	8kHz to 48kHz (Default)
0	0	1	Double Speed Mode	48kHz to 96kHz
0	1	0	Quad Speed Mode	96kHz to 192kHz

Table 2. System Clock Example in Manual Setting Mode

LRCK (kHz)	MCLK (MHz)						Sampling Speed Mode
f_S	128 × f_S	192 × f_S	256 × f_S	384 × f_S	512 × f_S	768 × f_S	
8.0	1.0240	1.5360	2.0480	3.0720	4.0960	6.1440	Normal Speed Mode
44.1	5.6448	8.4672	11.2896	16.9344	22.5792	N/A	Normal Speed Mode
48.0	6.1440	9.2160	12.2880	18.4320	24.5760	N/A	Normal Speed Mode
88.2	11.2896	16.9344	22.5792	N/A	N/A	N/A	Double Speed Mode
96.0	12.2880	18.4320	24.5760	N/A	N/A	N/A	Double Speed Mode
176.4	22.5792	N/A	N/A	N/A	N/A	N/A	Quad Speed Mode
192.0	24.5760	N/A	N/A	N/A	N/A	N/A	Quad Speed Mode

DETAILED DESCRIPTION (continued)

De-emphasis Filter

The SET4038 incorporates a digital de-emphasis filter, implemented as an IIR filter with a constant time (tC) of either 50μs or 15μs. Notably, this filter is exclusively compatible with the normal speed mode. It supports three distinct sampling frequencies (32kHz, 44.1kHz and 48kHz). Individual settings for each DAC, namely DAC1 (SDTI1), DAC2 (SDTI2), DAC3 (SDTI3) and DAC4 (SDTI4), allow for tailored de-emphasis configuration through register adjustments. This flexibility ensures that the SET4038 can accommodate a range of audio processing needs.

Table3. De-emphasis Filter Control

Mode	Sampling Speed Mode	DEM11 (DEM41-21)	DEM10 (DEM40-20)	DEM
0	Normal Speed Mode	0	0	44.1kHz
1	Normal Speed Mode	0	1	OFF (Default)
2	Normal Speed Mode	1	0	48kHz
3	Normal Speed Mode	1	1	32kHz

Audio Interface Format

During operation, it is advisable not to alter the TDM1-0 bits, DIF2-0 bits, SDS2-0 bits, TDM1-0 pins and DIF pin settings.

Normal Mode (TDM1-0 Bits = 00)

Audio data from eight channels is streamed into the SET4038 through the SDTI1-4 pins, utilizing the BICK and LRCK inputs for synchronization. The SDS2-0 bits serve to select the appropriate data stream. Furthermore, the device supports eight distinct data formats, which can be chosen by using the DIF2-0 bits as detailed inTable 4. This versatility allows for seamless integration with a wide range of audio sources and processing requirements. Regardless of the format, the serial data is always transmitted with the most significant bit (MSB) first, in 2's complement format, and is latched on the rising edge of BICK.

TDM128 Mode (TDM1-0 Bits = 01)

Audio data from eight channels is streamed into the SET4038 through the SDTI1-2 pins, utilizing the BICK and LRCK inputs for synchronization. The SDS2-0 bits serve to select the appropriate data stream. The inputs to the SDTI3-4 pins are disregarded during the data streaming process. The BICK frequency remains static at 128 × fS, providing a constant synchronization rate. Furthermore, the device supports six distinct data formats, which can be chosen by using the DIF2-0 bits as detailed in Table 4. Regardless of the format, the serial data is always transmitted with the most significant bit (MSB) first, in 2's complement format, and is latched on the rising edge of BICK.

TDM256 Mode (TDM1-0 Bits = 10)

Audio data from sixteen channels is streamed into the SET4038 through the SDTI1-2 pins, utilizing the BICK and LRCK inputs for synchronization. The SDS2-0 bits serve to select the appropriate data stream. The inputs to the SDTI3-4 pins are disregarded during the data streaming process. The BICK frequency remains static at 256 × fS, providing a constant synchronization rate. Furthermore, the device supports six distinct data formats, which can be chosen by using the DIF2-0 bits as detailed in Table 4. Regardless of the format, the serial data is always transmitted with the most significant bit (MSB) first, in 2's complement format, and is latched on the rising edge of BICK.

TDM512 Mode (TDM1-0 Bits = 11)

Audio data from sixteen channels is streamed into the SET4038 through the SDTI1 pin, utilizing the BICK and LRCK inputs for synchronization. The SDS2-0 bits serve to select the appropriate data stream. The inputs to the SDTI3-4 pins are disregarded during the data streaming process. The BICK frequency remains static at 512 × f_S, providing a constant synchronization rate. Furthermore, the device supports six distinct data formats, which can be chosen by using the DIF2-0 bits as detailed in Table 4. Regardless of the format, the serial data is always transmitted with the most significant bit (MSB) first, in 2's complement format, and is latched on the rising edge of BICK.

DETAILED DESCRIPTION (continued)

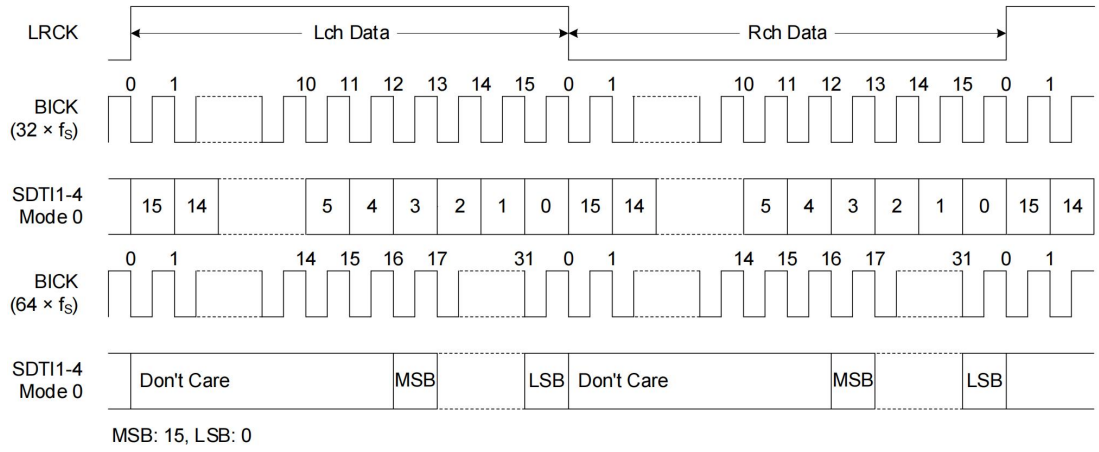
Table 4. Audio Data Format

Mode		TDM1	TDM0	DIF2	DIF1	DIF0	LRCK	BICK	SDTI Format
Normal (1)	0	0	0	0	0	0	H/L	≥ 32 × f_S	16-Bit LSB Justified
	1			0	0	1	H/L	≥ 40 × f_S	20-Bit LSB Justified
	2			0	1	0	H/L	≥ 48 × f_S	24-Bit MSB Justified
	3			0	1	1	L/H	32 × f_S	16-Bit I^2S Compatible
							L/H	≥ 48 × f_S	24-Bit I^2S Compatible
	4			1	0	0	H/L	≥ 48 × f_S	24-Bit LSB Justified
	5			1	0	1	H/L	≥ 64 × f_S	32-Bit LSB Justified
	6			1	1	0	H/L	≥ 64 × f_S	32-Bit MSB Justified
	7			1	1	1	L/H	≥ 64 × f_S	32-Bit I^2S Compatible
TDM128	–	0	1	0	0	0	↑	128 × f_S	N/A
	–			0	0	1	↑	128 × f_S	N/A
	8			0	1	0	↑	128 × f_S	24-Bit MSB Justified
	9			0	1	1	↓	128 × f_S	24-Bit I^2S Compatible
	10			1	0	0	↑	128 × f_S	24-Bit LSB Justified
	11			1	0	1	↑	128 × f_S	32-Bit LSB Justified
	12			1	1	0	↑	128 × f_S	32-Bit MSB Justified
	13			1	1	1	↓	128 × f_S	32-Bit I^2S Compatible
TDM256	–	1	0	0	0	0	↑	256 × f_S	N/A
	–			0	0	1	↑	256 × f_S	N/A
	14			0	1	0	↑	256 × f_S	24-Bit MSB Justified
	15			0	1	1	↓	256 × f_S	24-Bit I^2S Compatible
	16			1	0	0	↑	256 × f_S	24-Bit LSB Justified
	17			1	0	1	↑	256 × f_S	32-Bit LSB Justified
	18			1	1	0	↑	256 × f_S	32-Bit MSB Justified
	19			1	1	1	↓	256 × f_S	32-Bit I^2S Compatible
TDM512	–	1	1	0	0	0	↑	512 × f_S	N/A
	–			0	0	1	↑	512 × f_S	N/A
	20			0	1	0	↑	512 × f_S	24-Bit MSB Justified
	21			0	1	1	↓	512 × f_S	24-Bit I^2S Compatible
	22			1	0	0	↑	512 × f_S	24-Bit LSB Justified
	23			1	0	1	↑	512 × f_S	32-Bit LSB Justified
	24			1	1	0	↑	512 × f_S	32-Bit MSB Justified
	25			1	1	1	↓	512 × f_S	32-Bit I^2S Compatible

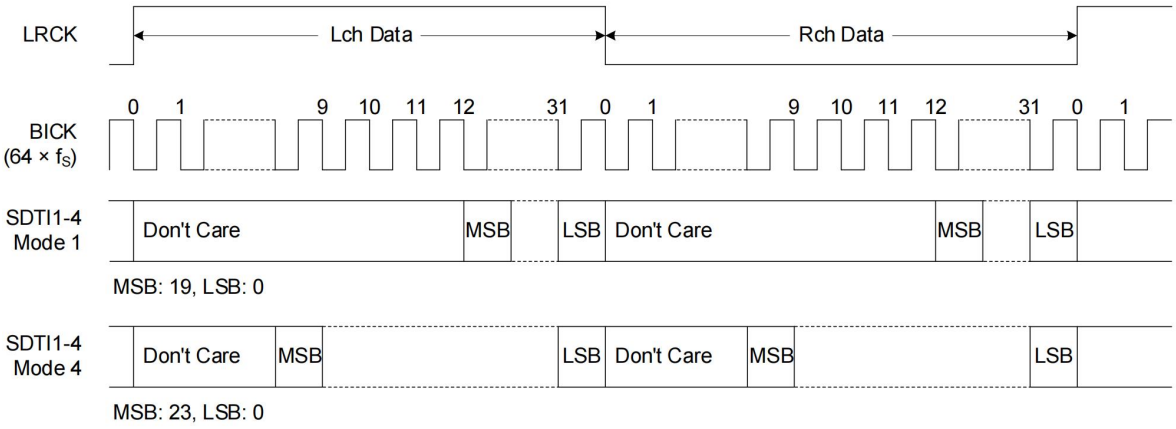
NOTE:

1. BICK refers to the requirement that the bit input to each channel must be greater than the length of setting format.

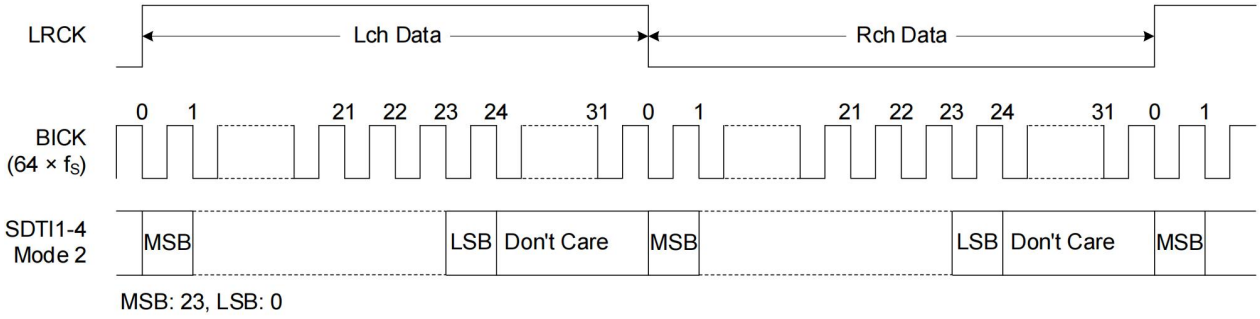
DETAILED DESCRIPTION (continued)



Audio Data Format Timing (Mode 0)

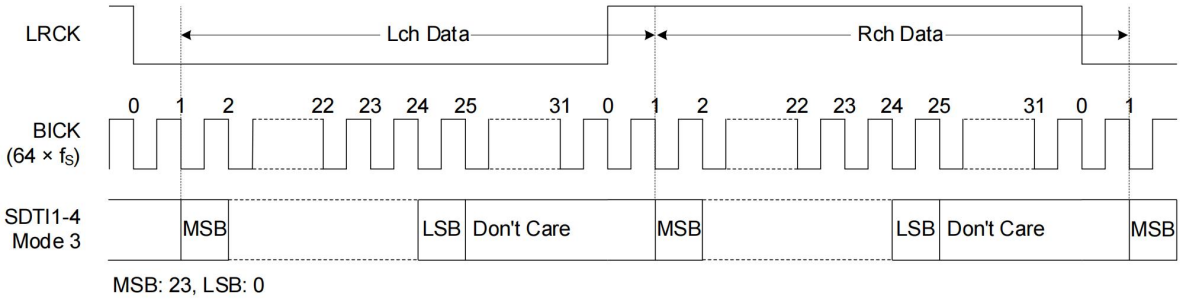


Audio Data Format Timing (Mode 1 and 4)

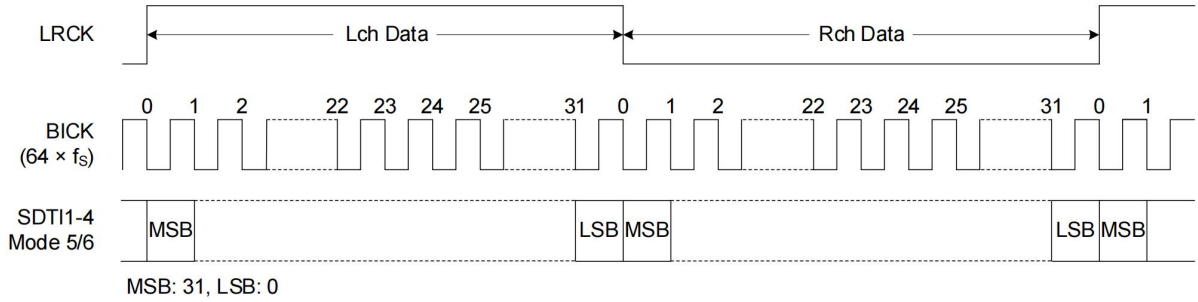


Audio Data Format Timing (Mode 2)

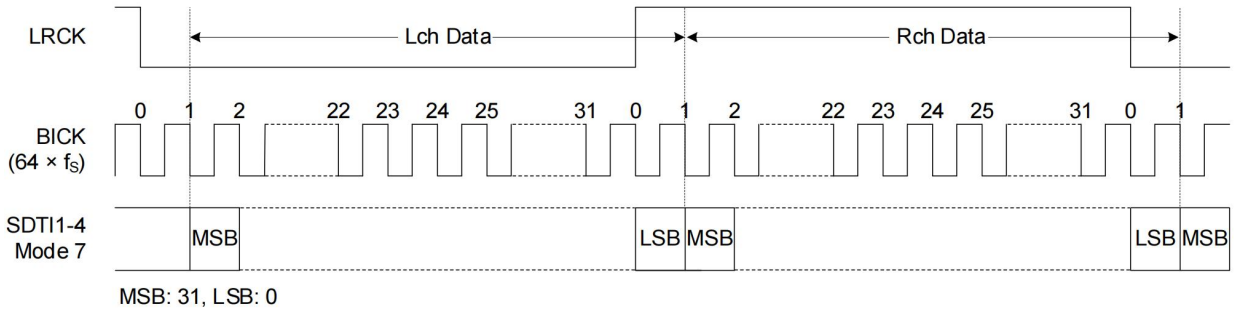
DETAILED DESCRIPTION (continued)



Audio Data Format Timing (Mode 3)

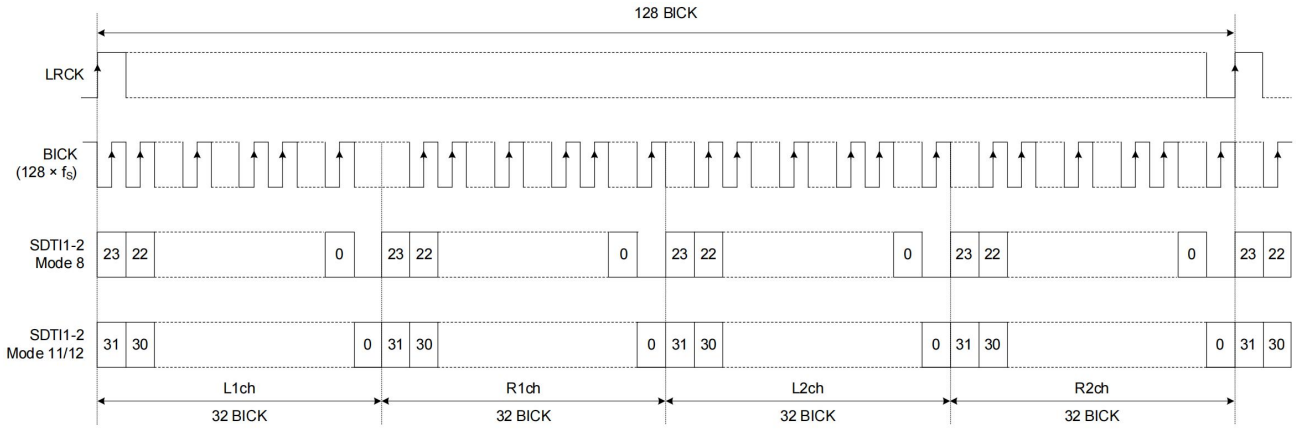


Audio Data Format Timing (Mode 5 and 6)

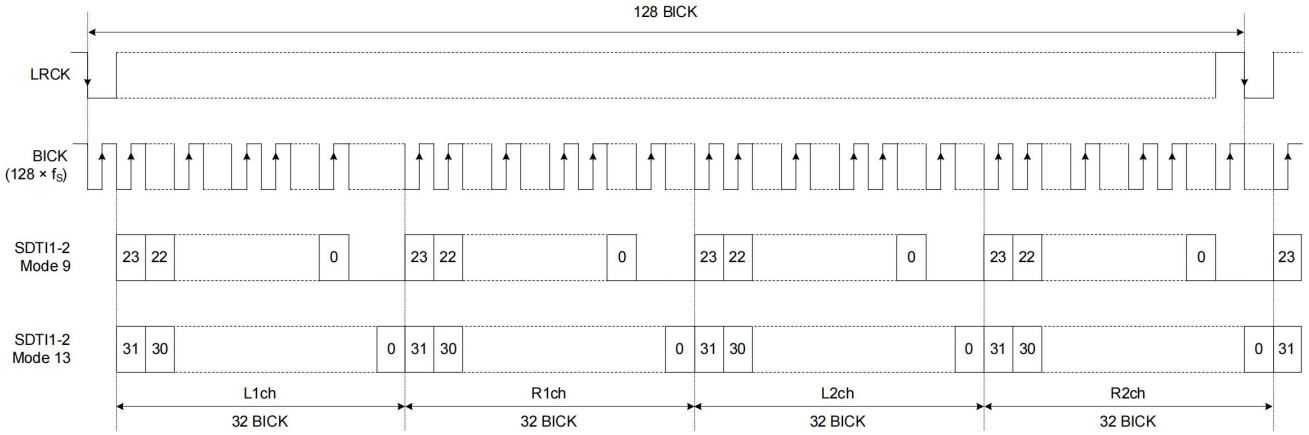


Audio Data Format Timing (Mode 7)

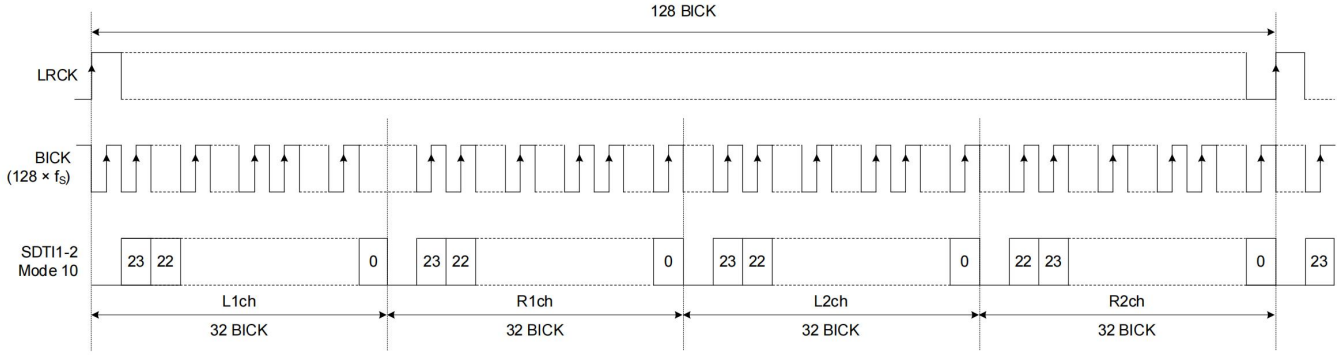
DETAILED DESCRIPTION (continued)



Audio Data Format Timing (Mode 8, 11 and 12)

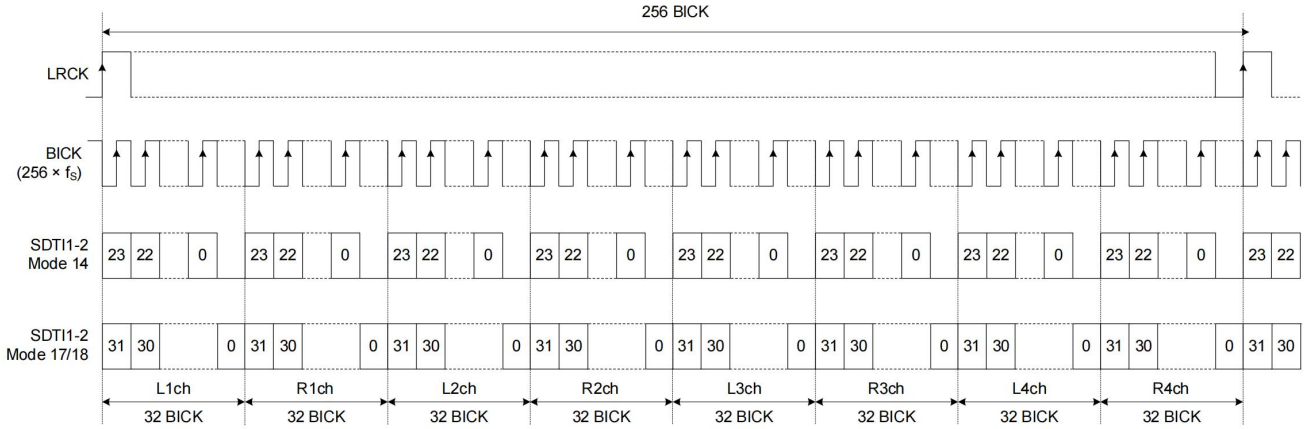


Audio Data Format Timing (Mode 9 and 13)

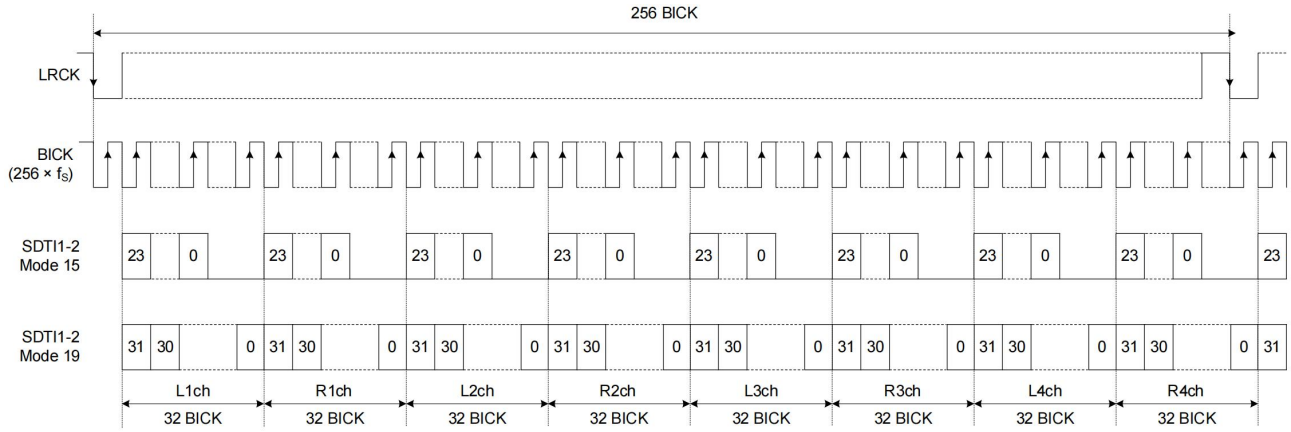


Audio Data Format Timing (Mode 10)

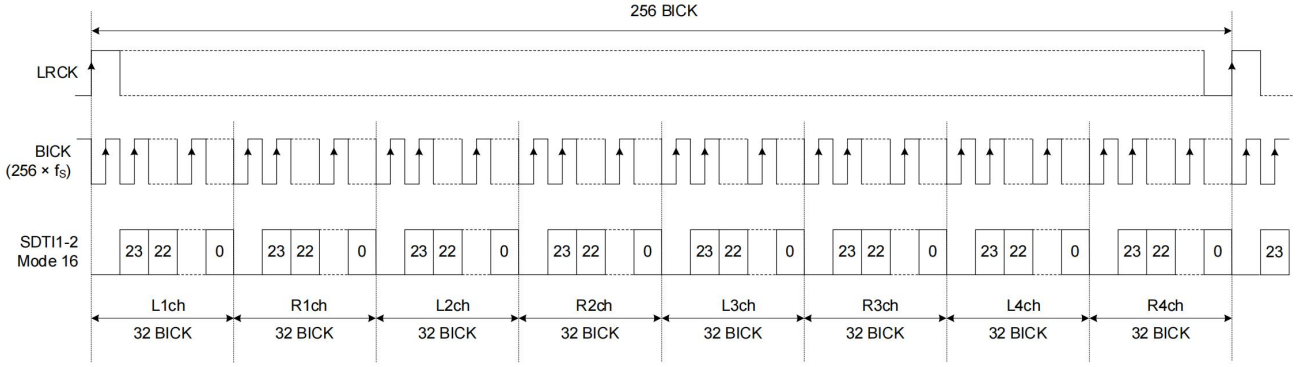
DETAILED DESCRIPTION (continued)



Audio Data Format Timing (Mode 14, 17 and 18)

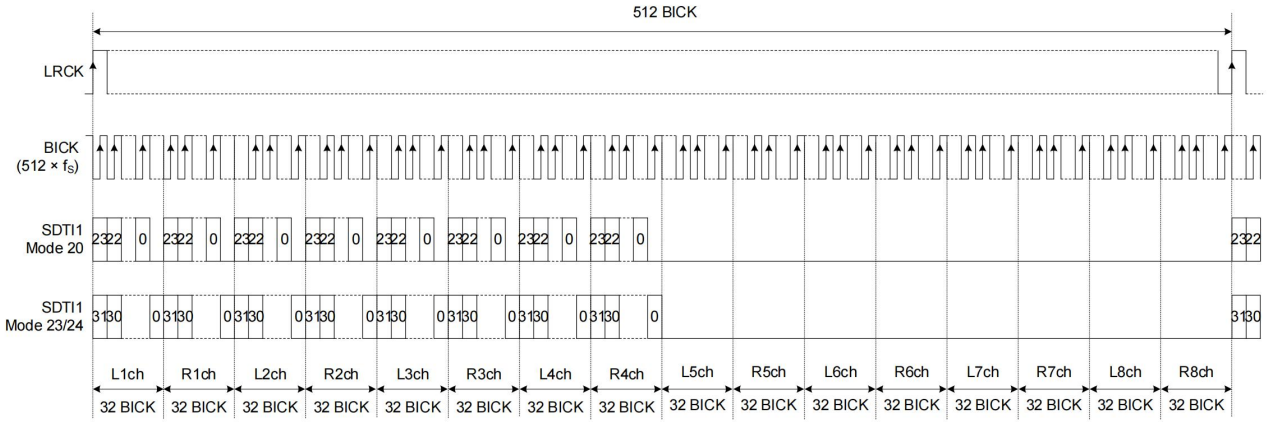


Audio Data Format Timing (Mode 15 and 19)

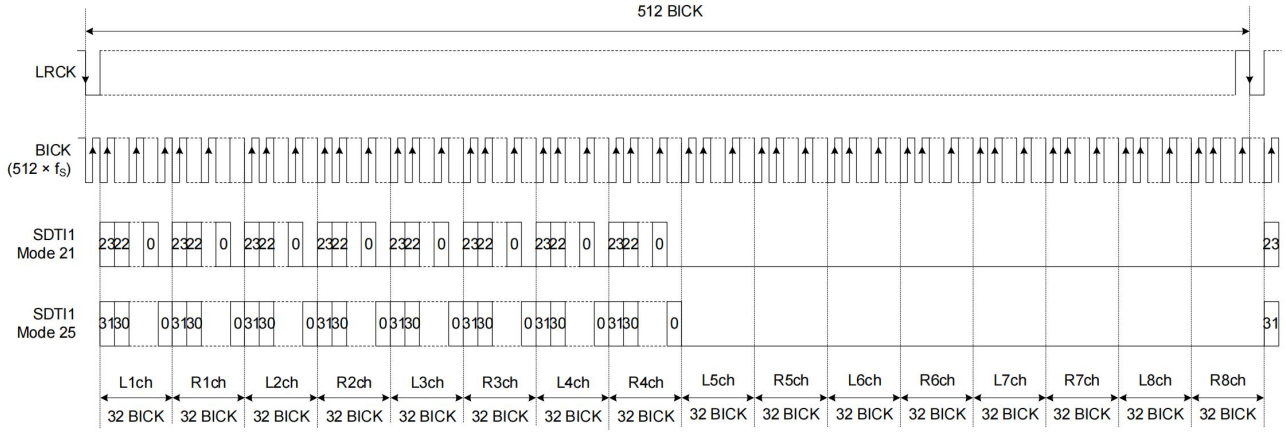


Audio Data Format Timing (Mode 16)

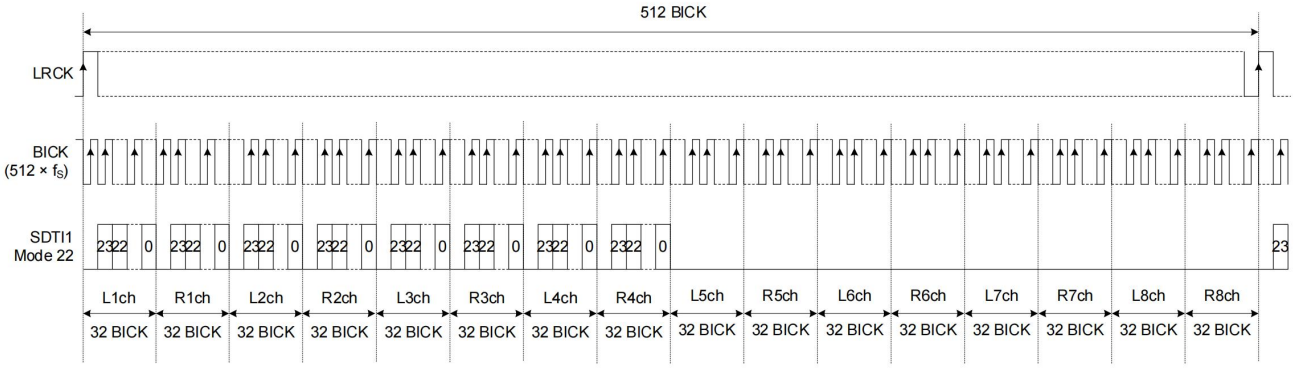
DETAILED DESCRIPTION (continued)



Audio Data Format Timing (Mode 20, 23 and 24)



Audio Data Format Timing (Mode 21 and 25)

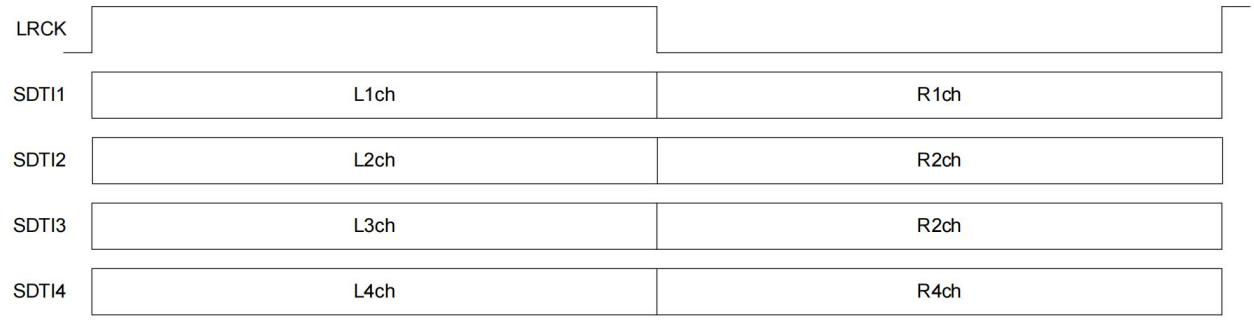


Audio Data Format Timing (Mode 22)

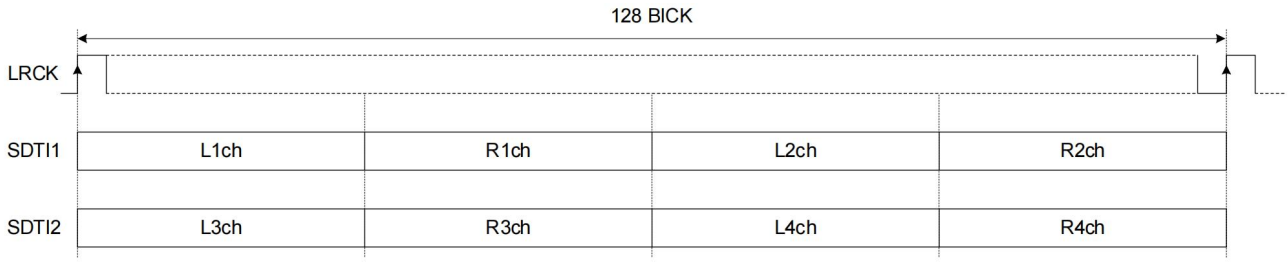
DETAILED DESCRIPTION (continued)

Data Select

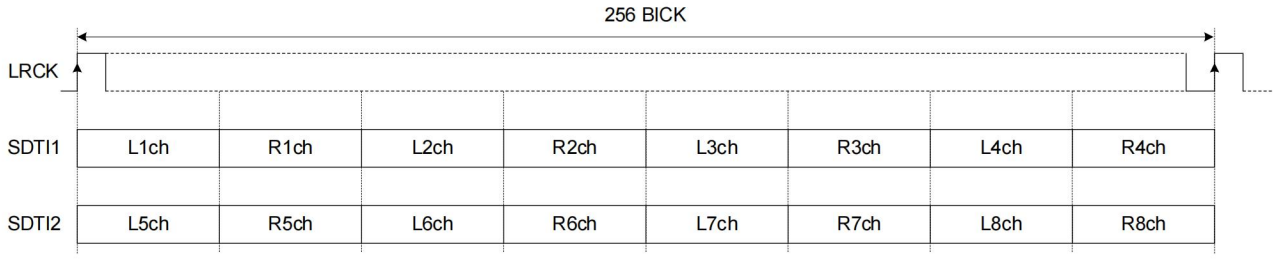
The playback channel of each DAC is controlled by SDS2-0 bits.



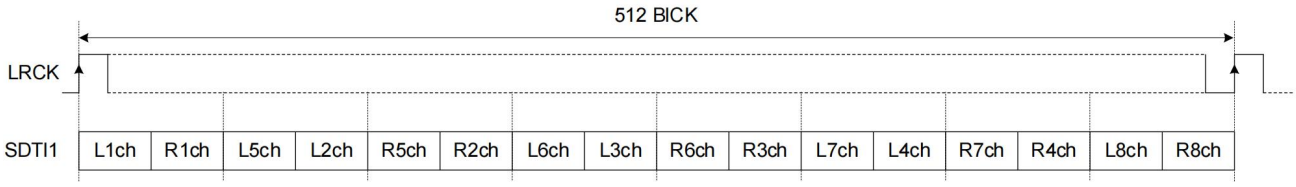
Normal Mode Data Slot



TDM128 Mode Data Slot



TDM256 Mode Data Slot



TDM512 Mode Data Slot

DETAILED DESCRIPTION (continued)

Table 5. Data Select (X: Do Not Care)

Made	SDS2	SDS1	SDS0	DAC1		DAC2		DAC3		DAC4	
				Lch	Rch	Lch	Rch	Lch	Rch	Lch	Rch
Normal	X	0	0	L1ch	R1ch	L2ch	R2ch	L3ch	R3ch	L4ch	R4ch
	X	0	1	L2ch	R2ch	L3ch	R3ch	L4ch	R4ch	L1ch	R1ch
	X	1	0	L3ch	R3ch	L4ch	R4ch	L1ch	R1ch	L2ch	R2ch
	X	1	1	L4ch	R4ch	L1ch	R1ch	L2ch	R2ch	L3ch	R3ch
TDM128	X	0	0	L1ch	R1ch	L2ch	R2ch	L3ch	R3ch	L4ch	R4ch
	X	0	1	L2ch	R2ch	L3ch	R3ch	L4ch	R4ch	L1ch	R1ch
	X	1	0	L3ch	R3ch	L4ch	R4ch	L1ch	R1ch	L2ch	R2ch
	X	1	1	L4ch	R4ch	L1ch	R1ch	L2ch	R2ch	L3ch	R3ch
TDM256	0	0	0	L1ch	R1ch	L2ch	R2ch	L3ch	R3ch	L4ch	R4ch
	0	0	1	L2ch	R2ch	L3ch	R3ch	L4ch	R4ch	L5ch	R5ch
	0	1	0	L3ch	R3ch	L4ch	R4ch	L5ch	R5ch	L6ch	R6ch
	0	1	1	L4ch	R4ch	L5ch	R5ch	L6ch	R6ch	L7ch	R7ch
	1	0	0	L5ch	R5ch	L6ch	R6ch	L7ch	R7ch	L8ch	R8ch
	1	0	1	L6ch	R6ch	L7ch	R7ch	L8ch	R8ch	L1ch	R1ch
	1	1	0	L7ch	R7ch	L8ch	R8ch	L1ch	R1ch	L2ch	R2ch
	1	1	1	L8ch	R8ch	L1ch	R1ch	L2ch	R2ch	L3ch	R3ch
TDM512	0	0	0	L1ch	R1ch	L2ch	R2ch	L3ch	R3ch	L4ch	R4ch
	0	0	1	L2ch	R2ch	L3ch	R3ch	L4ch	R4ch	L5ch	R5ch
	0	1	0	L3ch	R3ch	L4ch	R4ch	L5ch	R5ch	L6ch	R6ch
	0	1	1	L4ch	R4ch	L5ch	R5ch	L6ch	R6ch	L7ch	R7ch
	1	0	0	L5ch	R5ch	L6ch	R6ch	L7ch	R7ch	L8ch	R8ch
	1	0	1	L6ch	R6ch	L7ch	R7ch	L8ch	R8ch	L1ch	R1ch
	1	1	0	L7ch	R7ch	L8ch	R8ch	L1ch	R1ch	L2ch	R2ch
	1	1	1	L8ch	R8ch	L1ch	R1ch	L2ch	R2ch	L3ch	R3ch

The SET4038 incorporates a high-performance mode, which can be activated by adjusting specific combinations of LRCK, BICK and MCLK frequencies in conjunction with the DFS2-0 bits. In this mode, the THD + N dynamic performance parameters are enhanced. For detailed configuration relationships, please refer toTable 6below.

Table 6. Detailed Configuration of High-Performance Mode

High-Performance Mode				
Mode	**DFS2-0 Bits**	**LRCK (kHz)**	**BICK (MHz)**	**MCLK (MHz)**
Normal	001	48	3.072	12.288
TDM128	001	48	6.144	12.288
TDM256	001	48	12.288	12.288
TDM512	001	48	24.576	12.288
Normal	001	96	6.144	12.288
Normal	010	96	6.144	12.288
TDM128	001	96	12.288	12.288
TDM128	010	96	12.288	12.288
TDM256	001	96	24.576	12.288
TDM256	010	96	24.576	12.288

DETAILED DESCRIPTION (continued)

Digital Filter

Three distinct digital filters are offered for playback, offering a diverse range of sound hues to choose from . The selection of these digital filters is determined by the SLOW bit and the SSLOW bit.

Table 7. Digital Filter Setting

SSLOW Bit	SLOW Bit	Mode
0	0	Sharp Roll-Off Filter (Default)
0	1	Slow Roll-Off Filter
1	1	
1	0	Super Slow Roll-Off Mode

Zero Detection

The SET4038 boasts a unique feature of channel-independent zero detection. This functionality allows for the selection of zero detection channels, the AOUTL1-4 and AOUTR1-4 pins, through the control 5 and 6 registers (comprising the L1-4 bits and R1-4 bits). If the input data remains constantly at zero for 8192 consecutive LRCK cycles in any given channels, the DZF pin will switch to the high state. If the input data of each channel does not reach zero, the DZF pin will promptly revert to the low state. Additionally, when the RSTN bit is set to 0, the DZF pin of both channels will transition to high. However, when the RSTN bit returns to 1, the DZF pin of both channels will revert to low after approximately 4-5/f_S. Furthermore, the DZF bit allows for the inversion of the polarity of the DZF pin. It is worth noting that when RSTN bit is set to 1 if all channels are disabled, the outputs of the DZF pin will not be zero.

Table 8. DZF Pin Function

DZF Bit	DZF Pin	Data
0	Low	Not Zero (1)
0	High	Zero Detect (2)
1	High	Not Zero
1	Low	Zero Detect

NOTES:

1. Not zero: any one of the zero detection channels, which is established by L1-4 bits and R1-4 bits, fails to detect zero.
2. Zero detect: one of the zero detection channels configured through the L1-4 bits and R1-4 bits successfully detects the presence of zero.

Digital Volume Function

The SET4038 incorporates a digital attenuator that operates independently of any specific channel, offering 256 distinct attenuation levels with increments of 0.5dB. The attenuation level for each DAC4-1 can be individually configured by using the ATT7-0 bits located in register 03H, 04H, 0FH to 14H, as outlined inTable 9.

Table 9. Attenuation Level Applied by Digital Attenuator

ATT7-0 Bits (Register 03H, 04H, 0FH to 14H)	Attenuation Level
FFH	+0dB
FEH	-0.5dB
FDH	-1.0dB
…	…
02H	-126.5dB
01H	-127.0dB
00H	Mute (-∞)

DETAILED DESCRIPTION (continued)

The transition time between the set values of the ATT7-0 bits can be adjusted using the ATS1-0 bits, as detailed in Table 10. In modes 0, 1 and 2, the transition between set values is designed as a soft transition, effectively eliminating switching noise during the transition process.

Table 10. Transition Time for Digital Volume Adjustment

Mode	ATS1 Bit	ATS0 Bit	ATT Speed
0	0	0	4080/f_S (Default)
1	0	1	2040/f_S
2	1	0	510/f_S
3	1	1	255/f_S

In mode 0, the transition between set values occurs smoothly, spanning 4080 distinct levels. Completing the transition from FFH to 00H requires a duration of 4080/fS, which translates to approximately 85ms when the sampling frequency (fS) is set to 48kHz. Additionally, if the PDN pin is set to low, the ATT7-0 bits will automatically reset to FFH.

If a change is made to the digital volume while the reset is active, the volume will revert to the newly set value once the reset is released. If the volume is modified within 5/fS of the reset being lifted, the change will occur immediately without undergoing a soft transition.

LR Channel Output Signal Select

The SET4038s input and output signal combinations can be configured by using the MONO1-4 and SELLR1-4 bits.

Additionally, the phase of the DAC output signal can be controlled through the INVL1-4 and INVR1-4 bits. These settings are compatible with all audio formats supported by the SET4038.

Table 11. Selection of Output for DAC1

MONO1 Bit	SELLR1 Bit	INVL1 Bit	INVR1 Bit	L1ch Output	R1ch Output
0	0	0	0	L1ch Input	R1ch Input
		1	0	L1ch Input Invert	R1ch Input
		0	1	L1ch Input	R1ch Input Invert
		1	1	L1ch Input Invert	R1ch Input Invert
0	1	0	0	R1ch Input	L1ch Input
		1	0	R1ch Input Invert	L1ch Input
		0	1	R1ch Input	L1ch Input Invert
		1	1	R1ch Input Invert	L1ch Input Invert
1	0	0	0	L1ch Input	L1ch Input
		1	0	L1ch Input Invert	L1ch Input
		0	1	L1ch Input	L1ch Input Invert
		1	1	L1ch Input Invert	L1ch Input Invert
1	1	0	0	R1ch Input	R1ch Input
		1	0	R1ch Input Invert	R1ch Input
		0	1	R1ch Input	R1ch Input Invert
		1	1	R1ch Input Invert	R1ch Input Invert

DETAILED DESCRIPTION (continued)

Table 12. Selection of Output for DAC2

MONO2 Bit	SELLR2 Bit	INVL2 Bit	INVR2 Bit	L2ch Output	R2ch Output
0	0	0	0	L2ch Input	R2ch Input
		1	0	L2ch Input Invert	R2ch Input
		0	1	L2ch Input	R2ch Input Invert
		1	1	L2ch Input Invert	R2ch Input Invert
0	1	0	0	R2ch Input	L2ch Input
		1	0	R2ch Input Invert	L2ch Input
		0	1	R2ch Input	L2ch Input Invert
		1	1	R2ch Input Invert	L2ch Input Invert
1	0	0	0	L2ch Input	L2ch Input
		1	0	L2ch Input Invert	L2ch Input
		0	1	L2ch Input	L2ch Input Invert
		1	1	L2ch Input Invert	L2ch Input Invert
1	1	0	0	R2ch Input	R2ch Input
		1	0	R2ch Input Invert	R2ch Input
		0	1	R2ch Input	R2ch Input Invert
		1	1	R2ch Input Invert	R2ch Input Invert

Table 13. Selection of Output for DAC3

MONO3 Bit	SELLR3 Bit	INVL3 Bit	INVR3 Bi	L3ch Output	R3ch Output
0	0	0	0	L3ch Input	R3ch Input
		1	0	L3ch Input Invert	R3ch Input
		0	1	L3ch Input	R3ch Input Invert
		1	1	L3ch Input Invert	R3ch Input Invert
0	1	0	0	R3ch Input	L3ch Input
		1	0	R3ch Input Invert	L3ch Input
		0	1	R3ch Input	L3ch Input Invert
		1	1	R3ch Input Invert	L3ch Input Invert
1	0	0	0	L3ch Input	L3ch Input
		1	0	L3ch Input Invert	L3ch Input
		0	1	L3ch Input	L3ch Input Invert
		1	1	L3ch Input Invert	L3ch Input Invert
1	1	0	0	R3ch Input	R3ch Input
		1	0	R3ch Input Invert	R3ch Input
		0	1	R3ch Input	R3ch Input Invert
		1	1	R3ch Input Invert	R3ch Input Invert

DETAILED DESCRIPTION (continued)

Table 14. Selection of Output for DAC4

MONO4 Bit	SELLR4 Bit	INVL4 Bit	INVR4 Bit	L4ch Output	R4ch Output
0	0	0	0	L4ch Input	R4ch Input
		1	0	L4ch Input Invert	R4ch Input
		0	1	L4ch Input	R4ch Input Invert
		1	1	L4ch Input Invert	R4ch Input Invert
0	1	0	0	R4ch Input	L4ch Input
		1	0	R4ch Input Invert	L4ch Input
		0	1	R4ch Input	L4ch Input Invert
		1	1	R4ch Input Invert	L4ch Input Invert
1	0	0	0	L4ch Input	L4ch Input
		1	0	L4ch Input Invert	L4ch Input
		0	1	L4ch Input	L4ch Input Invert
		1	1	L4ch Input Invert	L4ch Input Invert
1	1	0	0	R4ch Input	R4ch Input
		1	0	R4ch Input Invert	R4ch Input
		0	1	R4ch Input	R4ch Input Invert
		1	1	R4ch Input Invert	R4ch Input Invert

LDO Protection Function

SET4038 integrates an LDO internally, which provides separate clean power supply to key modules inside the chip. This LDO supports over-current protection (OCP) function, which is a current limiting OCP. The typical OCP threshold value is 80mA. When the LDO load current exceeds the OCP threshold, the OCP circuit will forcibly clamp the output current to 80mA. If the load continues to increase at this time, the LDO output current will still remain at around 80mA, but the LDO output voltage (LDOO) will continue to decrease until it reaches 0. The typical LDOO value is 1.85V. Once the chip malfunctions, it is recommended that users first check whether LDOO voltage is normal. If the LDOO voltage is found to be below 1.5V or above 2.2V, it is recommended to restart the chip through the PDN pin. Note that in principle, the LDO only supplies power to the internal circuits of SET4038 and does not supply power to board level devices.

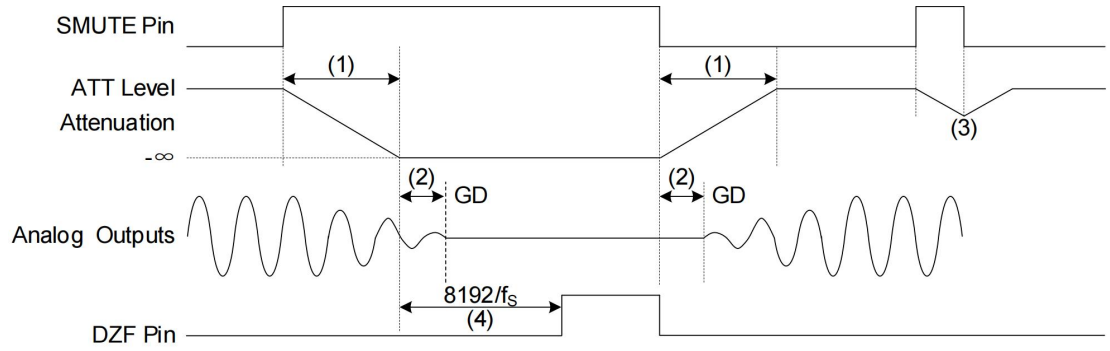
Table 15. LDO Fault Detection

LDO Fault Type	LDO Fault Conditions
LDO Over-Current Threshold	LDO Output Current: 80mA (TYP)
LDO Under-Voltage Threshold	LDO Output Voltage: 1.5V (TYP)
LDO Over-Voltage Threshold	LDO Output Voltage: 2.2V (TYP)

DETAILED DESCRIPTION (continued)

Soft Mute Operation

The soft mute function operates exclusively within the digital domain. The SMUTE pin is responsible for controlling the soft mute operation, as depicted in Function for Soft Mute and Detection of Zero Signal. Whenever the SMUTE pin is set to high or the SMUTE bit is configured as 1, the output signal experiences an attenuation of negative infinity during the ATT_DATA × ATT transition period, commencing from the current ATT level. When the SMUTE pin is brought back to low or the SMUTE bit is reset to 0, and the output attenuation gradually transitions back to the ATT level over the same ATT_DATA × ATT transition time. When the soft mute is scrapped before the attenuation reaches negative infinity, the attenuation process halts immediately, and the signal returns to the ATT level within the same ATT_DATA × ATT transition time cycle. The soft mute feature is advantageous when it comes to switching signal sources without interrupting the signal transmission, as it ensures a smooth transition with minimal audio disruption.



NOTES:

1. The transition time for ATT_DATA × ATT is determined by the specific value of ATT_DATA. For instance, when ATT_DATA is set to 255 in the normal speed mode, the transition time spans 4080 LRCK cycles.
2. Each digital input corresponds to an analog output that exhibits a certain group delay (GD).
3. If the soft mute function is deactivated prior to attaining the negative infinity attenuation level after initiating the operation, the attenuation process will be aborted, and the volume will revert to the previous ATT level within the same transition cycle.
4. If the input data for the zero detection channel remains constantly zeros for a duration of 8192 LRCK cycles, the DZF pin transitions to the high state. If the input data ceases to be zero, the DZF pin promptly returns to the low state.

Function for Soft Mute and Detection of Zero Signal

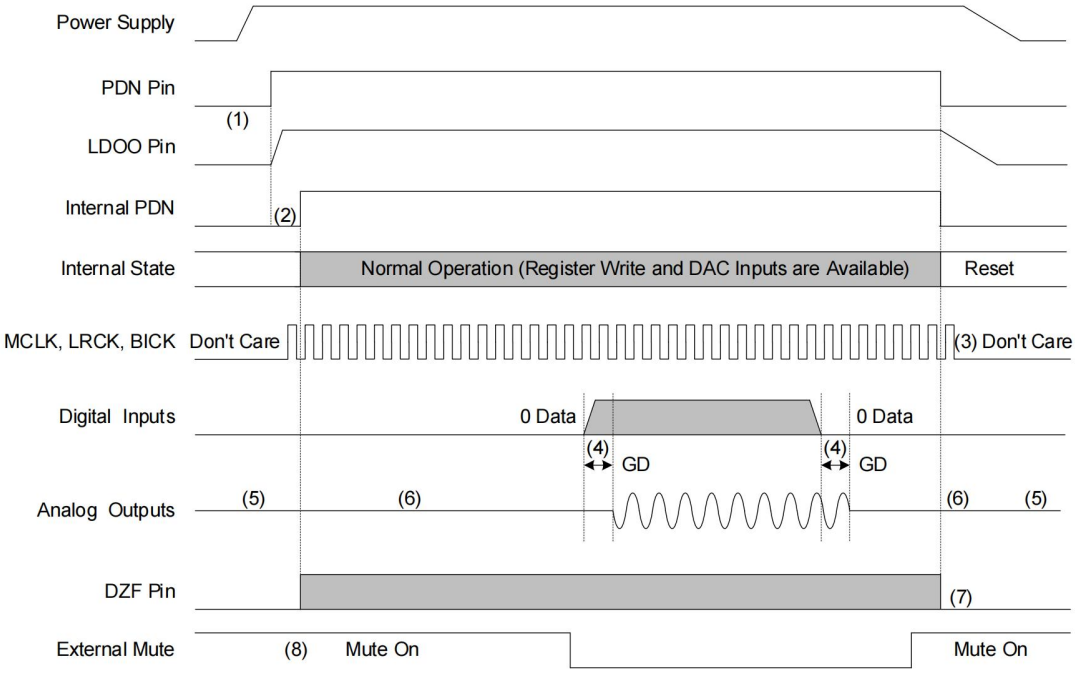
System Reset

Upon power-up, the SET4038 should be initially reset by setting the PDN pin to low. This reset ensures that the device starts in a known and consistent state. The PDN pin must be set to high to deactivate the power-down state of the reference voltages, including LDO and VCOM. The settings will take effect within 1ms after the power-down state is lifted. The SET4038 remains in a power-down state until both the MCLK (master clock) and LRCK (left/right clock) inputs are present and active. This ensures that the device does not commence operation until the necessary clock signals are available and stable, preventing potential issues due to incomplete or unstable initialization.

DETAILED DESCRIPTION (continued)

Power-Down Function

When the PDN pin of the SET4038 is set to low, the device enters power-down mode, resulting in the analog outputs entering a floating (Hi-Z) state. The specific timings for both power-up and power-down operations are detailed in Figure 9.



NOTES:

1. After AVDD and TVDD have been successfully powered up, it is recommended to maintain the PDN pin at low for a duration of 800ns to ensure a stable and reliable transition into the operational state of the device.
2. Once the PDN pin is set to high, the internal LDO and VCOM will activate, initiating the power-up process. Subsequently, the internal registers will undergo initialization. Once the PDN pin is set to high, register writing becomes available within 1ms. This brief delay ensures that the SET4038 has stabilized and is ready to accept configuration and control commands through its registers. During this period, the device performs internal initialization procedures necessary for proper operation.
3. The MCLK, BICK and LRCK clocks can be deactivated in the power-down mode (when the PDN pin is set to low).
4. Each digital input corresponds to an analog output that exhibits a certain group delay (GD).
5. During the power-down mode, the analog outputs enter a floating state (Hi-Z).
6. When the PDN signal experiences an edge transition, click noise may occur. This noise regardless of whether 0 data is input.
7. In the internal power-down mode, the DZF output pin is low.
8. In the case that click noise 5 has an impact on system performance, external analog outputs are recommended to be muted. Figure 9 refers to the timing example.

Figure 9. Example of Pin Power-Up and Power-Down Sequence

DETAILED DESCRIPTION (continued)

Power-Off and Reset Functions

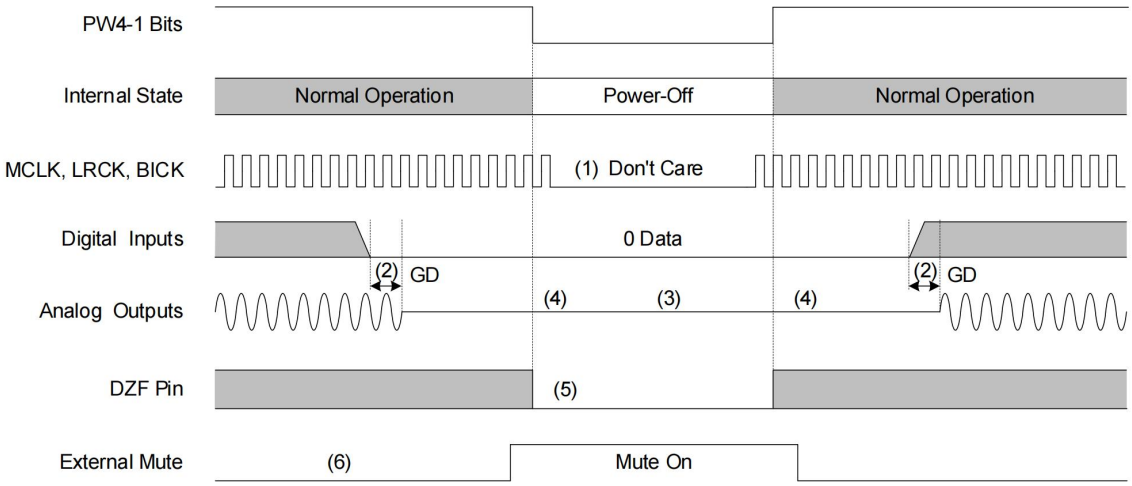
Table 16. Power-Off and Reset Functions

RSTN Bit	PW4-1 Bits	Analog Output			
		DAC4	DAC3	DAC2	DAC1
0	0000	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0001	Hi-Z	Hi-Z	Hi-Z	VCOM
0	0010	Hi-Z	Hi-Z	VCOM	Hi-Z
0	0011	Hi-Z	Hi-Z	VCOM	VCOM
0	0100	Hi-Z	VCOM	Hi-Z	Hi-Z
0	0101	Hi-Z	VCOM	Hi-Z	VCOM
0	0110	Hi-Z	VCOM	VCOM	Hi-Z
0	0111	Hi-Z	VCOM	VCOM	VCOM
0	1000	VCOM	Hi-Z	Hi-Z	Hi-Z
0	1001	VCOM	Hi-Z	Hi-Z	VCOM
0	1010	VCOM	Hi-Z	VCOM	Hi-Z
0	1011	VCOM	Hi-Z	VCOM	VCOM
0	1100	VCOM	VCOM	Hi-Z	Hi-Z
0	1101	VCOM	VCOM	Hi-Z	VCOM
0	1110	VCOM	VCOM	VCOM	Hi-Z
0	1111	VCOM	VCOM	VCOM	VCOM
1	0000	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0001	Hi-Z	Hi-Z	Hi-Z	Normal
1	0010	Hi-Z	Hi-Z	Normal	Hi-Z
1	0011	Hi-Z	Hi-Z	Normal	Normal
1	0100	Hi-Z	Normal	Hi-Z	Hi-Z
1	0101	Hi-Z	Normal	Hi-Z	Normal
1	0110	Hi-Z	Normal	Normal	Hi-Z
1	0111	Hi-Z	Normal	Normal	Normal
1	1000	Normal	Hi-Z	Hi-Z	Hi-Z
1	1001	Normal	Hi-Z	Hi-Z	Normal
1	1010	Normal	Hi-Z	Normal	Hi-Z
1	1011	Normal	Hi-Z	Normal	Normal
1	1100	Normal	Normal	Hi-Z	Hi-Z
1	1101	Normal	Normal	Hi-Z	Normal
1	1110	Normal	Normal	Normal	Hi-Z
1	1111	Normal	Normal	Normal	Normal

DETAILED DESCRIPTION (continued)

Power-Off Function (PW4-1 Bits)

All DAC4-1 can be immediately powered down by configuring the PW4-1 bits to 0000. During the internal power-down mode, the transition of analog outputs gets into a floating state (Hi-Z). Additionally, the DACs are reset, and the digital block is powered down by configuring the RSTN bit to 0. In the reset state, when the DAC is energized and the necessary clock signals (MCLK, LRCK and BICK) are provided, the analog outputs the VCOM voltage level (Table 16). It is important to note that setting the PW4-1 bits does not initialize the internal register values, it simply controls the power state of the DACs. Figure 10 exhibits a sample timing diagram depicting the process of powering on and powering down the device.



NOTES:

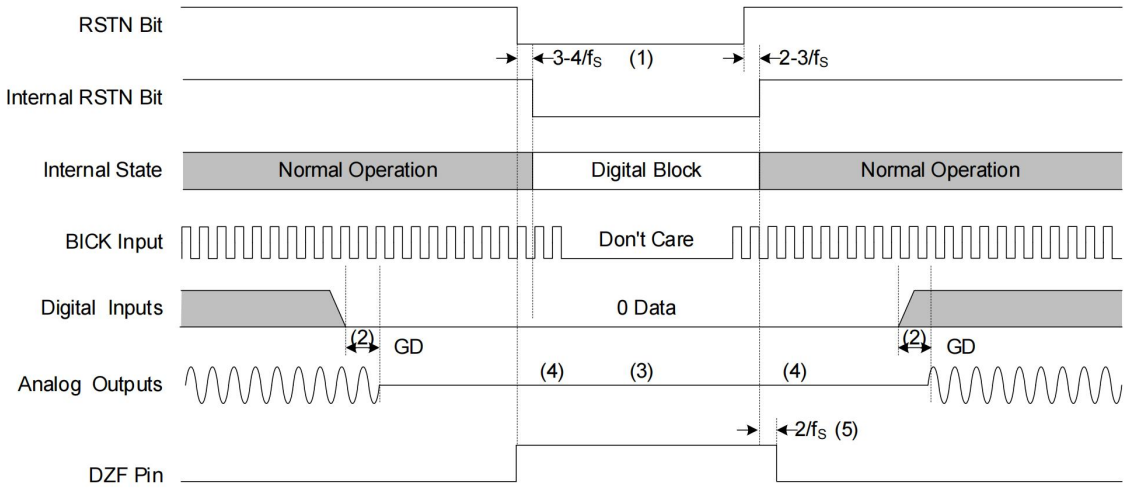
1. The MCLK, BICK and LRCK clocks can be deactivated in the power-down mode (PW4-1 bits = 0000).
2. Each digital input corresponds to an analog output that exhibits a certain group delay (GD).
3. During the power-down mode, the analog outputs enter a floating state (Hi-Z).
4. The rising and falling edges (↓ ↑) of the internal clock timing for the PW4-1 bits produce click noise, regardless of whether 0 data is inputted or not.
5. In the internal power-down mode, the DZF pin outputs low (PW4-1 bits = 0000).
6. In the case that click noise 3 has a negative impact on system performance, external analog outputs are recommended to be muted.

Figure 10. Example of Pin Power-Up and Power-Down Sequence

DETAILED DESCRIPTION (continued)

Reset Function (RSTN Bit)

The DAC can be reset by setting RSTN bit to 0 but this action does not automatically revert the internal registers to their default settings. During this period, the DZF pin will emit high signal whenever clocks (MCLK, BICK and LRCK) are received as inputs. As an illustration,Figure 11depicts a sample reset sequence triggered by the RSTN bit.



NOTES:

1. There is a delay of 3-4/f_S from when the RSTN bit transitions to 0 until the internal RSTN bit also reaches 0. Similarly, there is a delay of 2-3/f_S from when the RSTN bit transitions to 0 until the internal RSTN bit reaches 1.

2. Each digital input corresponds to an analog output that exhibits a certain group delay (GD).

3. During the power-down mode, the analog outputs VCOM voltage.

4. The rising and falling edges (↓ ↑) of the internal clock timing for the PW4-1 bits produce click noise, regardless of whether 0 data is inputted or not.

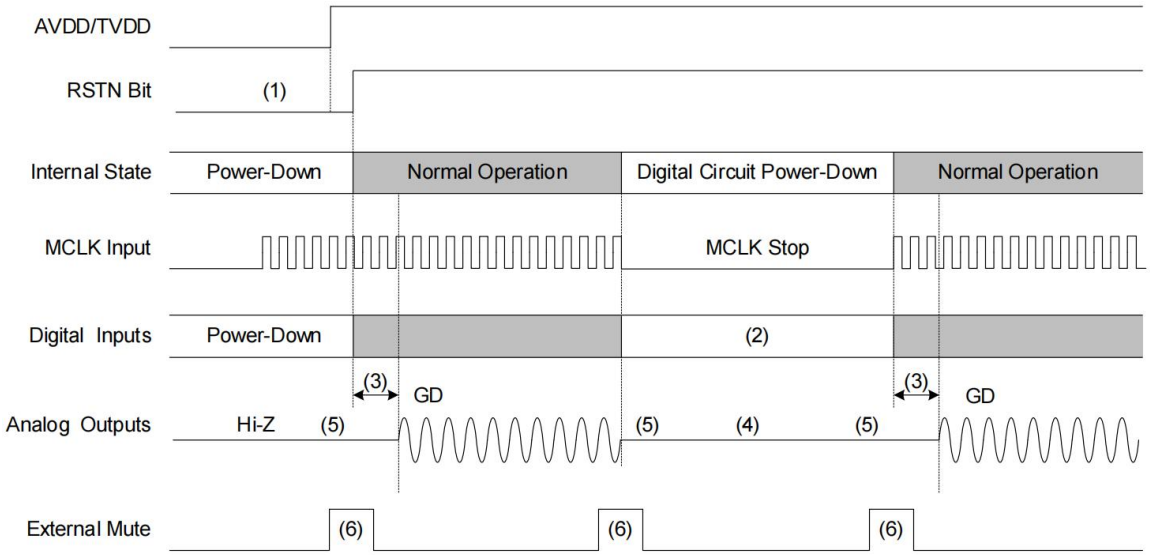
5. When the RSTN bit transitions from high to low, the DZF pin changes its state to high. Subsequently, after the internal RSTN experiences a rising edge, the DZF pin transitions to low after a duration of 2/f_S.

Figure 11. Example of Reset Sequence

DETAILED DESCRIPTION (continued)

Reset Function (MCLK)

The SET4038 automatically enters a reset state when the MCLK is halted during normal operation, provided that the PDN pin is set to high. Under such conditions, the analog outputs transition to VCOM voltage. When the MCLK (master clock) is re-input, the SET4038 exits the reset state and resumes its operational functions. When MCLK is stopped, zero detect function is disabled.



NOTES:

1. After AVDD and TVDD have been successfully powered up, it is recommended to maintain the PDN pin at low for a duration of 800ns to ensure a stable and reliable transition into the operational state of the device.

2. Data of digital inputs can be stopped. Inputting 0 data during the pause period can effectively mitigate the click noise that would otherwise occur upon the subsequent resumption of the MCLK input.

3. Each digital input corresponds to an analog output that exhibits a certain group delay (GD).

4. When the MCLK signal is paused, the analog outputs VCOM voltage.

5. Click noise emerges within a duration of 3 to 4 LRCK cycles, commencing from the rising edge of the PDN pin or MCLK input. It is worth noting that this noise still exists when the input data is 0.

6. In the case that click noise 3 has a negative impact on system performance, external analog outputs are recommended to be muted.Figure 12 exhibits the sample timing diagram.

Figure 12. Example of Reset Sequence 2

Parallel Mode

By configuring the I2C pin to high and the PS pin to high, the parallel mode becomes accessible. In this operational mode, the register settings are disregarded. Instead, the audio interface format and soft mute function are directly controlled through designated pins. As for other functionalities, they operate according to the default settings programmed within the registers. The system clock is always set to operate in auto-setting mode in parallel mode.

Audio Interface

In parallel mode, the audio interface format is exclusively controlled by the TDM1-0 and DIF pins (Table 17). In parallel mode, both the zero detection function and the functionalities configured through registers are not operational. This means that in parallel mode, the audio interface format is determined solely by physical pins , while other advanced features offered by register settings are unavailable.

DETAILED DESCRIPTION (continued)

Table 17. Parallel Mode

Pin			Mode
TDM1	TDM0	DIF	
0	0	0	Mode 6
0	0	1	Mode 7
0	1	0	Mode 12
0	1	1	Mode 13
1	0	0	Mode 18
1	0	1	Mode 19
1	1	0	Mode 24
1	1	1	Mode 25

Serial Control Interface

The functions of SET4038 are managed through registers, which can be programmed by using two types of

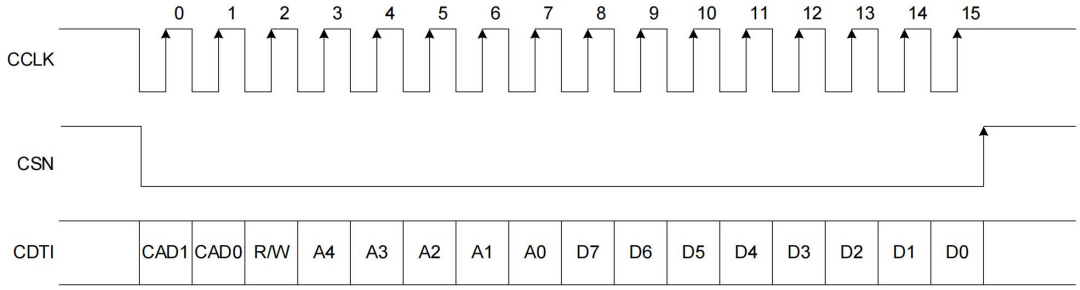
control modes. In the 3-wire serial control mode, the internal registers are regulated when the I2C pin is set to low and the PS pin is also set to low. Alternatively, when the I^2C pin is set to high and the PS pin remains at low, the registers are controlled in the I2C-bus control mode. CAD1-0 pins can determine the chip address.

To initialize the internal registers, simply set the PDN pin to low. When the RSTN bit is set to 0, the internal timing circuit undergoes a reset. However, it is important to note that this action does not initialize the register values. The registers retain their previous settings, and only the timing circuit is affected by this reset operation. When the PDN pin is at low, writing to the registers is not possible.

3-Wire Serial Control Mode (I^2C Pin = Low)

Utilizing the 3-wire control interface pins of CCLK, CSN and CDTI, the internal registers can be written. The data transmitted over this interface consists of a 2-bit chip address, a fixed 1-bit read/write flag set exclusively for writing, a register address (starting with the MSB, spanning 5 bits), and control data (also starting with the MSB, totaling 8 bits). Data is latched once CSN transitions from low to high. The input of both the address and data occurs on the rising edge of CCLK, while data output happens on the falling edge. The highest clock frequency of CCLK is 5MHz, which determines the upper limit for the rate of data transfer.

To initialize the internal registers, the PDN pin must be set to low. In serial mode, the internal timing circuit can be reset by assigning the RSTN bit a value of 0, but register values are not initialized.



NOTES:

1. CAD1, CAD0: chip slave address
2. R/W: read/write (write only)
3. A4 to A0: register address
4. D7 to D0: control data

Figure 13. Command of 3-Wire Serial Control Timing

DETAILED DESCRIPTION (continued)

I2C Serial Interface and Data Communication

Standard I2C interface is used to program SET4038 parameters and get status reports. I2C is well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SET4038 operates as a slave device that address is 0x20. It has twenty-one 8-bit registers, numbered from REG0x00 to REG0x14.

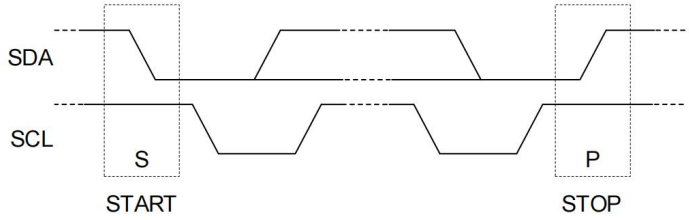
Physical Layer

The standard I2C interface of SET4038 supports standard mode and fast mode communication speeds. The frequency of stand mode is up to 100kHz, while the fast mode is up to 400kHz. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

I^2C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in I^2C Bus in START and STOP Conditions. All transactions begin by the master who applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high-to-low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.



I^2C Bus in START and STOP Conditions

Data Bit Transmission and Validity

Data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by the master. Bit transfer in I2C is shown in Figure 14.

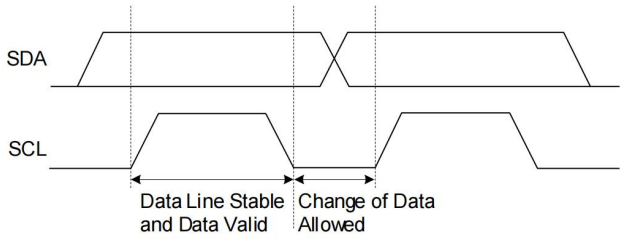


Figure 14. I^2C Bus Bit Transfer

DETAILED DESCRIPTION (continued)

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the most significant bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 14 shows the byte transfer process with I2C interface.

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of **each** byte by transmitter, an acknowledge bit is replied by the receiver as ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte has been received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including for the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse, and the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either STOP (P) to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

I^2C-Bus Control Mode (I2C Pin = High)

The SET4038 supports the fast mode I^2C-bus (maximum: 400kHz).

Write Operations

Figure 15 shows the data transfer sequence of the I2C-bus mode. The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/W). R/W bit is 0 for a write transaction and 1 for read (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction) .

After the START condition, the first byte (Figure 15) consists of the chip slave address of the SET4038. The address consists of 7 bits followed by an eighth bit designated as the data direction bit (R/W). The first five most significant bits of the slave address are permanently set to 00100. The subsequent bits, CAD1-0 serve as device address bits, uniquely identifying a specific device on the bus. These device address bits are configured through dedicated hard-wired input pins (CAD1, CAD0) as shown in Figure 16. When the slave address matches the address of the SET4038, the device generates an acknowledgement, initiating the execution of the corresponding operation. The master to generate the acknowledge-related clock pulse and release the SDA line to a high state during the acknowledge clock pulse, as illustrated in Figure 15. An R/W bit value of 1 signifies the execution of a read operation, while a value of 0 indicates a write operation.

The second byte comprises the control register address to the SET4038. This format follows the rule of MSB first, and the most significant 3 bits are fixed to zeros (Figure 17).

The subsequent data, following the second byte, consists of control data in the format of MSB first, 8 bits (Figure 18). The SET4038 generates an acknowledgement upon receiving each byte. The data transfer process is always

concluded with a STOP condition initiated by the master. This STOP condition is defined by a low-to-high transition on the SDA line while SCL remains high (Figure 14).

DETAILED DESCRIPTION (continued)

The SET4038 is capable of executing multiple byte write operations within a single sequence. Upon receiving the third byte, the SET4038 generates an acknowledgment signal, indicating successful receipt, and subsequently waits for the next data to be transmitted. The master can continue to send additional bytes rather than terminate the write cycle after transmitting the first data byte. As each data packet is received, the internal address counter automatically increments by one, ensuring that the next data is stored in the consecutive address. If the address surpasses 14H before a stop condition is triggered, the address counter resets to 00H, leading to the overwriting of previous data. Therefore, it is essential to manage the data flow and stop condition carefully to avoid data error. It is worth noting that the R4ch ATT register cannot be written to individually. Instead, it must be written through a multi-byte write operation to ensure proper functionality.

During the high state period of the clock, the data on the SDA line must maintain stability. The state of the data line, whether high or low, can only be altered when the clock signal on the SCL line is in its low state, with exceptions being the START and STOP conditions (I2C Bus in START and STOP Conditions).

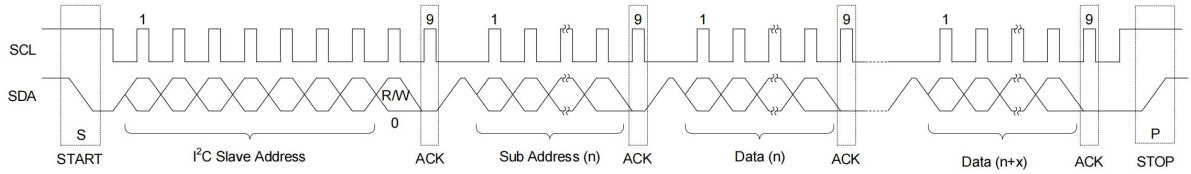


Figure 15. Data Transfer Sequence at the I²C-Bus Mode (Write)

0	0	1	0	0	CAD1	CAD0	R/W

NOTE: CAD1 and CAD0 can be controlled by pin settings.

Figure 16. Chip Slave Address

0	0	0	A4	A3	A2	A1	A0

Figure 17. Sub Address

D7	D6	D5	D4	D3	D2	D1	D0

Figure 18. Byte Data after the Sub Address

Read Operations

To initiate a read operation for the SET4038, the R/W bit should be set to 1. The master can acknowledge receipt and initiate a read operation for the subsequent address after successfully transmitting data, instead of concluding the write cycle upon receiving the first data word. When each data packet is received, the internal address counter automatically increments by one, and the next data automatically enters the next address. If the address exceeds 14H before the stop condition is generated, the address counter will reset to 00H, resulting in the reading of data from address 00H. The SET4038 can allow two fundamental read operations, namely current address read and random address read.

The SET4038 incorporates an internal address counter that keeps track of the address of the last accessed word and automatically increments it by one. Consequently, the subsequent read operation for the current address would retrieve data from address n + 1, assuming the previous access (read or write) was directed to address. Once the SET4038 receives the slave address with the R/W bit set to 1, the SET4038 generates an acknowledgement, transmits a single byte of data from the address designated by the internal address counter, and then increments the internal address counter by1.Ifthe master does not generate an acknowledgement but instead triggers a stop condition, the SET4038 will halt its transmission process.

DETAILED DESCRIPTION (continued)

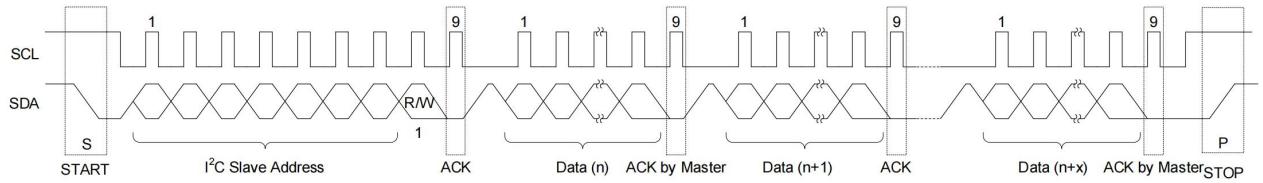


Figure 19. Data Transfer Sequence at the I²C-Bus Mode (Current Address Read)

The random read operation enables the master to randomly access any memory location. Before initializing a slave address and setting the R/W bit to 1, the master must i implement the operation of virtual write. This involves the master sending a start request, followed by the slave address with the R/W bit set to 0, and subsequently the desired register address for reading. Once the register address is acknowledged, the master promptly repeats the start request and transmits the slave address with the R/W bit set to 1. Upon receiving this sequence, the SET4038 responds an acknowledgement by transmitting a single byte of data from the specified address, and incrementing the internal address counter by one.If the master opts not to generate an acknowledgement but instead triggers a stop condition, the SET4038 will halt its transmission, as previously mentioned.

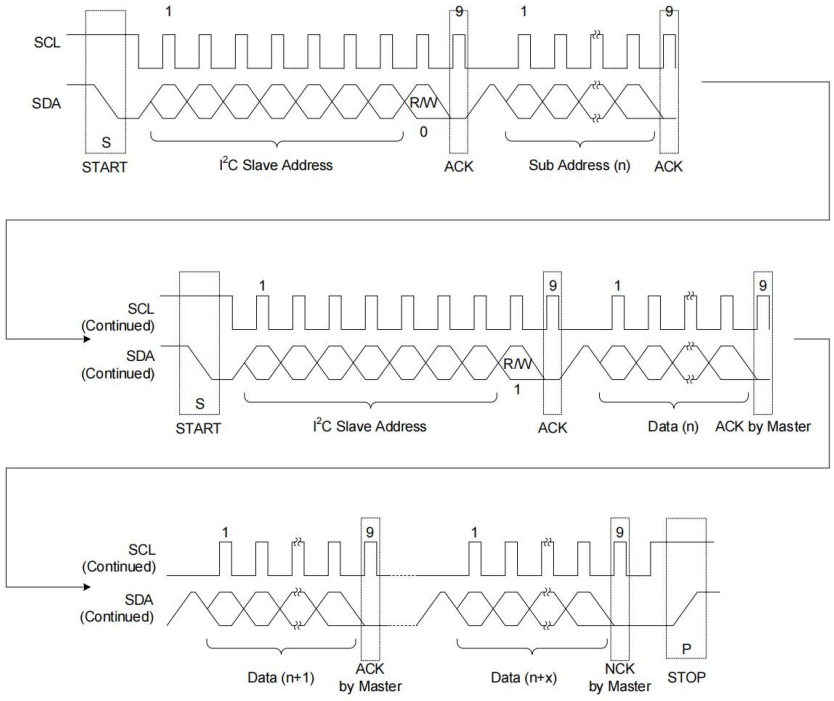


Figure 20. Data Transfer Sequence at the I²C-Bus Mode (Random Address Read)

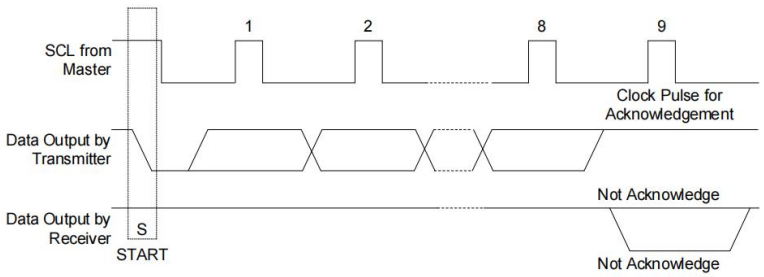


Figure 21. Acknowledge on the I²C-Bus

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB) .

Bit Types:

R/W: Read/Write

I²C Register Address Map

Address	Register Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00H	Control 1	0	0	0	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	1	DFS1	DFS0	DEM11	DEM10	SMUTE
02H	Control 3	0	0	0	0	MONO1	DZFB	SELLR1	SLOW
03H	L1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	R1ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	Control 4	INVL1	INVR1	INVL2	INVR2	SELLR2	0	DFS2	SSLOW
06H	Reserved	–	–	–	–	–	–	–	–
07H	Control 5	R2	R4	L3	L1	0	0	0	1
08H	Control 6	R1	R3	L2	L4	0	0	0	0
09H	Reserved	–	–	–	–	–	–	–	–
0AH	Control 7	TDM1	TDM0	SDS1	SDS2	PW2	PW1	DEM21	DEM20
0BH	Control 8	ATS1	ATS0	0	SDS0	PW4	PW3	0	0
0CH	Control 9	INVR4	INVL4	INVR3	INVL3	0	0	0	0
0DH	Control 10	MONO	MONO3	MONO2	0	SELLR4	SELLR3	0	0
0EH	Control 11	DEM41	DEM40	DEM31	DEM30	0	0	0	0
0FH	L2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
10H	R2ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
11H	L3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
12H	R3ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
13H	L4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
14H	R4ch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

NOTES:

1. Addresses ranging from 15H to 1FH are not writable.

2. When designated as 0, the bit must be assigned a value of zero.

3. Upon setting the PDN pin to low, the registers undergo initialization and adopt their default values.

4. Upon setting the RSTN bit to 0, the internal timing is reset, whereas the registers maintain their current state without undergoing initialization.

REGISTER MAPS (continued)

REG0x00: Control 1 Register [Reset = 0x0D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3]	DIF2	1	R/W	Audio Data Interface Modes (Table 4) DIF2-0 default: 110 (mode 6: 32-bit MSB justified)
D[2]	DIF1	1	R/W	
D[1]	DIF0	0	R/W	
D[0]	RSTN	1	R/W	Internal Timing Reset 0 = Reset (when the DZF pin is set to high, the register values are uninitialized.) 1 = Normal operation (default)

REG0x01: Control 2 Register [Reset = 0x22]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	001	R/W	Reserved
D[4]	DFS1	0	R/W	Sampling Speed Mode Control (Table 1) DFS2-0 000 = Normal speed mode (default) 001 = Double speed mode 010 = Quad speed mode Others = N/A When adjusting the DFS2-0 bit setting, a click noise is generated.
D[3]	DFS0	0	R/W	
D[2]	DEM11	0	R/W	De-emphasis Response for DAC1 (Table 3) DEM11-10 00 = 44.1kHz 01 = OFF (default) 10 = 48kHz 11 = 32kHz
D[1]	DEM10	1	R/W	
D[0]	SMUTE	0	R/W	Soft Mute Enable 0 = Normal operation (default) 1 = Soft-muted of DAC outputs

REG0x02: Control 3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3]	MONO1	0	R/W	Upon setting the MONO1 bit to 1,the DAC1 transitions to MONO output mode.(Table 11) 0 = Stereo mode (default) 1 = MONO mode
D[2]	DZFB	0	R/W	Inverting Enable of DZF (Table 8) 0 = DZF pin set to high at zero detection (default) 1 = DZF pin set to low at zero detection
D[1]	SELLR1	0	R/W	Data Selection of DAC1 (Table 11) 0 = Normal mode (default) 1 = Swap mode This bit enables or disables the channel swapping feature. When set to 0, the audio system operates in normal mode, where the left channel input is routed to the left channel output, and the right channel input is routed to the right channel output. When set to 1, the audio system enters swap mode, where the left channel input is routed to the right channel output, and the right channel input is routed to the left channel output.
D[0]	SLOW	0	R/W	Slow Roll-Off Filter Enable (Table 7) 0 = Disable (default) 1 = Enable

REGISTER MAPS (continued)

REG0x03: L1chATT Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ATT7	1	R/W	Attenuation Level (Table 9) 1111 1111 = 0dB (default) 1111 1110 = -0.5dB … 0000 0001 = -127dB 0000 0000 = Mute (-∞)
D[6]	ATT6	1	R/W	
D[5]	ATT5	1	R/W	
D[4]	ATT4	1	R/W	
D[3]	ATT3	1	R/W	
D[2]	ATT2	1	R/W	
D[1]	ATT1	1	R/W	
D[0]	ATT0	1	R/W	

REG0x04: R1chATT Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ATT7	1	R/W	Attenuation Level (Table 9) 1111 1111 = 0dB (default) 1111 1110 = -0.5dB … 0000 0001 = -127dB 0000 0000 = Mute (-∞)
D[6]	ATT6	1	R/W	
D[5]	ATT5	1	R/W	
D[4]	ATT4	1	R/W	
D[3]	ATT3	1	R/W	
D[2]	ATT2	1	R/W	
D[1]	ATT1	1	R/W	
D[0]	ATT0	1	R/W	

REG0x05: Control 4 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	INVL1	0	R/W	Output of AOUTL1 Phase Inverting Enable Bit (Table 11) 0 = Normal (default) 1 = Inverted
D[6]	INVR1	0	R/W	Output of AOUTR1 Phase Inverting Enable Bit (Table 11) 0 = Normal (default) 1 = Inverted
D[5]	INVL2	0	R/W	Output of AOUTL2 Phase Inverting Enable Bit (Table 12) 0 = Normal (default) 1 = Inverted
D[4]	INVR2	0	R/W	Output of AOUTR2 Phase Inverting Enable Bit (Table 12) 0 = Normal (default) 1 = Inverted
D[3]	SELLR2	0	R/W	Data Selection of DAC2 (Table 12) 0 = Normal mode (default) 1 = Swap mode This bit enables or disables the channel swapping feature. When set to 0, the audio system operates in normal mode, where the left channel input is routed to the left channel output, and the right channel input is routed to the right channel output. When set to 1, the audio system enters swap mode, where the left channel input is routed to the right channel output, and the right channel input is routed to the left channel output.
D[2]	Reserved	0	R/W	Reserved
D[1]	DFS2	0	R/W	Sampling Speed Mode Control (Table 1) DFS2-0 000 = Normal speed mode (default) 001 = Double speed mode 010 = Quad speed mode Others = N/A When adjusting the DFS2-0 bit setting, a click noise is generated.
D[0]	SSLOW	0	R/W	Super Slow Roll-Off Mode Enable (Table 7) 0 = Disable (default) 1 = Enable

REGISTER MAPS (continued)

REG0x07: Control 5 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	R2	0	R/W	Zero Detect Flag Enable Bit for the DZF Pin 0 = Disable (default) 1 = Enable
D[6]	R4	0	R/W	
D[5]	L3	0	R/W	
D[4]	L1	0	R/W	
D[3:0]	Reserved	0001	R/W	Reserved

REG0x08: Control 6 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	R1	0	R/W	Zero Detect Flag Enable Bit for the DZF Pin 0 = Disable (default) 1 = Enable
D[6]	R3	0	R/W	
D[5]	L2	0	R/W	
D[4]	L4	0	R/W	
D[3:0]	Reserved	0000	R/W	Reserved

REG0x0A: Control 7 Register [Reset = 0x0D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	TDM1	0	R/W	TDM Mode Select TDM1-0 00 = Normal mode (default) 01 = TDM128 mode 10 = TDM256 mode 11 = TDM512 mode
D[6]	TDM0	0	R/W	
D[5]	SDS1	0	R/W	Data Selection for DAC1-4 0 = Normal operation (default) 1 = Output other slot data (Table 5) SDS2-0 default: 000
D[4]	SDS2	0	R/W	
D[3]	PW2	1	R/W	Power-Down Control for DAC2 0 = DAC2 power-off 1 = DAC2 power-on (default)
D[2]	PW1	1	R/W	Power-Down Control for DAC1 0 = DAC1 power-off 1 = DAC1 power-on (default)
D[1]	DEM21	0	R/W	De-emphasis Response for DAC2 DEM21-20 00 = 44.1kHz 01 = OFF (default) 10 = 48kHz 11 = 32kHz
D[0]	DEM20	1	R/W	

REGISTER MAPS (continued)

REG0x0B: Control 8 Register [Reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ATS1	0	R/W	Transition Time between Value Settings of ATT7-0 Bits (Table 10) ATS1-0 00 = 4080/f_S (default) 01 = 2040/f_S 10 = 510/fS11 = 255/f_S
D[6]	ATS0	0	R/W	
D[5]	Reserved	0	R/W	Reserved
D[4]	SDS0	0	R/W	Data Selection for DAC1-4 0 = Normal operation (default) 1 = Output other slot data (Table 5) SDS2-0 default: 000
D[3]	PW4	1	R/W	Power-Down Control for DAC4 0 = DAC4 power-off 1 = DAC4 power-on (default)
D[2]	PW3	1	R/W	Power-Down Control for DAC3 0 = DAC3 power-off 1 = DAC3 power-on (default)
D[1:0]	Reserved	00	R/W	Reserved

REG0x0C: Control 9 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	INVR4	0	R/W	Output of AOUTR4 Phase Inverting Enable Bit (Table 14) 0 = Normal (default) 1 = Inverted
D[6]	INVL4	0	R/W	Output of AOUTL4 Phase Inverting Enable Bit (Table 14) 0 = Normal (default) 1 = Inverted
D[5]	INVR3	0	R/W	Output of AOUTR3 Phase Inverting Enable Bit (Table 13) 0 = Normal (default) 1 = Inverted
D[4]	INVL3	0	R/W	Output of AOUTL3 Phase Inverting Enable Bit (Table 13) 0 = Normal (default) 1 = Inverted
D[3:0]	Reserved	0000	R/W	Reserved

REGISTER MAPS (continued)

REG0x0D: Control 10 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	MONO4	0	R/W	Upon setting the MONO4 bit to 1,the DAC4 transitions to MONO output mode. (Table 14) 0 = Stereo mode (default) 1 = MONO mode
D[6]	MONO3	0	R/W	Upon setting the MONO3 bit to 1,the DAC3 transitions to MONO output mode. (Table 13) 0 = Stereo mode (default) 1 = MONO mode
D[5]	MONO2	0	R/W	Upon setting the MONO2 bit to 1,the DAC2 transitions to MONO output mode. (Table 12) 0 = Stereo mode (default) 1 = MONO mode
D[4]	Reserved	0	R/W	Reserved
D[3]	SELLR4	0	R/W	Data Selection of DAC4 (Table 14) 0 = Normal mode (default) 1 = Swap mode This bit enables or disables the channel swapping feature. When set to 0, the audio syste operates in normal mode, where the left channel input is routed to the left channel output, and the right channel input is routed to the right channel output. When set to 1, the audio system enters swap mode, where the left channel input is routed to the right channel output, and the right channel input is routed to the left channel output.
D[2]	SELLR3	0	R/W	Data Selection of DAC3 (Table 13) 0 = Normal mode (default) 1 = Swap mode This bit enables or disables the channel swapping feature. When set to 0, the audio system operates in normal mode, where the left channel input is routed to the left channel output, and the right channel input is routed to the right channel output. When set to 1, the audio system enters swap mode, where the left channel input is routed to the right channel output, and the right channel input is routed to the left channel output.
D[1:0]	Reserved	00	R/W	Reserved

REG0x0E: Control 11 Register [Reset = 0x50]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	DEM41	0	R/W	De-emphasis Response for DAC4 (Table 3) DEM41-40 00 = 44.1kHz 01 = OFF (default) 10 = 48kHz 11 = 32kHz
D[6]	DEM40	1	R/W	
D[5]	DEM31	0	R/W	De-emphasis Response for DAC3 (Table 3) DEM31-30 00 = 44.1kHz 01 = OFF (default) 10 = 48kHz 11 = 32kHz
D[4]	DEM30	1	R/W	
D[3:0]	Reserved	0000	R/W	Reserved
D[1:0]	Reserved	00	R/W	Reserved

REG0x0F/0x11/0x13: L2ch/L3ch/L4chATT Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ATT7	1	R/W	Attenuation Level (Table 9) 1111 1111 = 0dB (default) 1111 1110 = -0.5dB … 0000 0001 = -127dB 0000 0000 = Mute (-∞)
D[6]	ATT6	1	R/W	
D[5]	ATT5	1	R/W	
D[4]	ATT4	1	R/W	
D[3]	ATT3	1	R/W	
D[2]	ATT2	1	R/W	
D[1]	ATT1	1	R/W	
D[0]	ATT0	1	R/W	

REGISTER MAPS (continued)

REG0x10/0x12/0x14: R2ch/R3ch/ R4chATT Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	ATT7	1	R/W	Attenuation Level (Table 9) 1111 1111 = 0dB (default) 1111 1110 = -0.5dB … 0000 0001 = -127dB 0000 0000 = Mute (-∞)
D[6]	ATT6	1	R/W	
D[5]	ATT5	1	R/W	
D[4]	ATT4	1	R/W	
D[3]	ATT3	1	R/W	
D[2]	ATT2	1	R/W	
D[1]	ATT1	1	R/W	
D[0]	ATT0	1	R/W	

APPLICATION INFORMATION

The SET4038 needs to input the MCLK signal in advance to execute the 3-wire serial/I2C-bus program. It can only enter its normal operating state once the power-up sequences for AVDD, TVDD and VREFH are completed, and the functional and digital logic blocks are enabled. It is crucial that the voltage at the digital input pins is synchronized with the voltage of TVDD to prevent reverse current flow, commonly known as back flow.

Grounding and Power Supply Decoupling

The SET4038 necessitates meticulous attention to its power supply and grounding configurations. AVDD and TVDD are usually sourced from the analog power supply. In cases where AVDD and TVDD are supplied independently, the specific power-up sequence between them is not crucial. For VSS1 and VSS2, they ought to be interconnected to a unified analog ground plane. It is essential to separate the analog ground from its digital ground and connect them as closely as possible to the point where the power supplies are introduced onto the printed circuit board. Positioning decoupling capacitors as close as possible to the SET4038 is imperative.

Voltage Reference

The analog output range is determined by the differential voltage between the VREFH and VREFL pins, with the VREFH pin typically connected to AVDD and the VREFL pin linked to VSS2. To mitigate the impact of high-frequency noise, it is recommended to connect VREFH and VREFL with a 0.1μF ceramic capacitor and a 10μF electrolytic capacitor, positioning them as close as possible to the respective pins.

VCOM is defined as the signal ground of the chip, and can output a voltage of AVDD × 1/2. To mitigate the impact of high-frequency noise, a 2.2μF ± 50% ceramic capacitor should be placed between the VCOM pin and VSS2, and it is crucial to position this capacitor as close to the pin as possible. It is important to note that no load current should be drawn from the VCOM pin. Additionally, it is essential to keep all signals, particularly clocks, away from the VREFH pin and the VCOM pin to prevent unwanted coupling into the SET4038.

The LDOO produces 1.2V, which serves as the voltage source for the internal digital circuit. To ensure the stability of the internal LDO, it is necessary to connect a 2.2μF±50% ceramic capacitor between the LDOO pin and VSS1, positioning it as close to the pin as possible. It is crucial to note that no load current should be drawn from the VCOM pin.

Analog Output

Nominally, the output signal range is centered on the VCOM voltage and spans 0.86 × VREFH Vpp.

The DAC employs a 2's complement data format, with a positive full-scale output corresponding to 7FFFFFFFH (for 32-bit) and a negative full-scale output corresponding to 80000000H (for 32-bit). The ideal output is VCOM voltage for 00000000H (for 32-bit).

To minimize noise generated by the delta-sigma modulator of the DAC beyond the audio pass-band in single-ended input mode, internal analog filters are employed. However, it's worth noting that the DAC outputs typically have DC offsets of a few millivolts relative to the VCOM voltage. Consequently, an external capacitor is normally used to eliminate this DC component. Unused input or output pins must be connected correctly. AOUTL1-4, AOUTR1-4 and DZF pins must be set to open and SDTI1-4 pins must be connected to VSS1.

APPLICATION INFORMATION (continued)

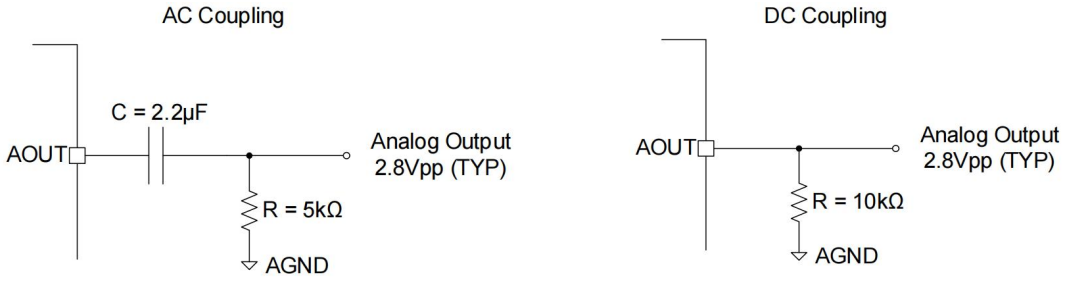
External Circuits of Analog Output

The analog output of this circuit typically reaches 2.8Vpp (as specified for the SET4038 model). Typically, due to the presence of DC offsets in the DAC outputs, which amount to a few millivolts relative to the VCOM voltage, an external capacitor is employed to eliminate the DC component. The cutoff frequency of the high-pass filter (HPF) is detailed in the following section.

$$f_C = 1/(2 \times \pi \times R \times C)\ (Hz) \qquad (1)$$

The external AC coupling capacitor is denoted by C, while R represents the load resistance. Given that C equals 2.2μF and R equals 5kΩ , the resulting cutoff frequency f_C is calculated to be 14.5Hz. Note that in AC coupling mode, the maximum resistive load capacity is 5kΩ .

Another output mode is DC coupling, as shown on the right side of Example of Output Buffer Circuits. The output is directly connected to the load without AC coupling capacitor. In this mode, there is a common mode voltage at the output terminal, which is AVDD/2 (typical value is 1.65V), and the maximum resistive load capacity is 10kΩ .



Example of Output Buffer Circuits

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

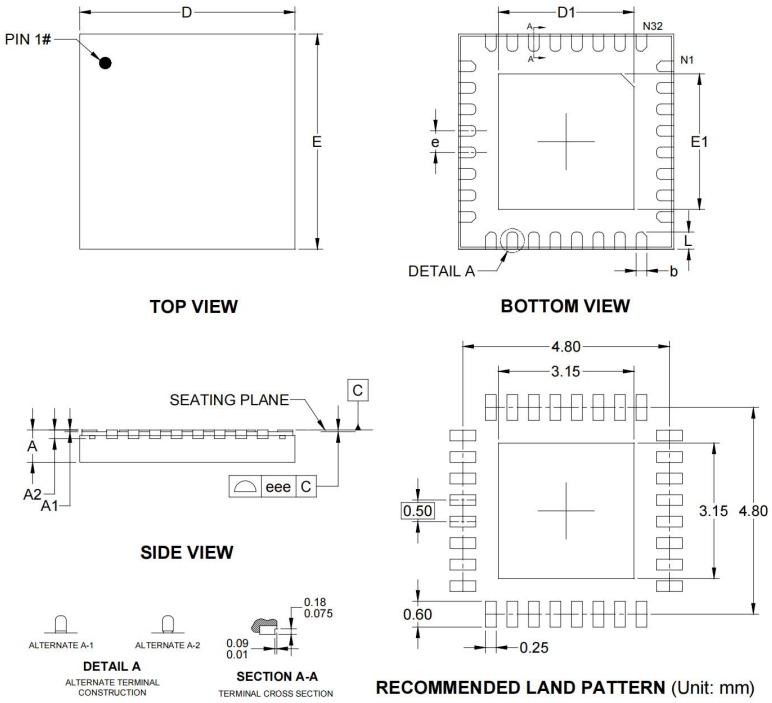
This integrated circuit can be damaged if ESD protections are not considered carefully. SET recommends that all

integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SET reserves the right to make any change in circuit design, or specifications without prior notice.

PACKAGE TQFN-5×5-32FL



Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
D	4.900	-	5.100
E	4.900	-	5.100
D1	3.050	-	3.250
E1	3.050	-	3.250
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

NOTES:This drawing is subject to change without notice.

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