

## General Description

The SLD609S is a low noise, high PSRR, fast transient response, and low dropout voltage linear regulator which is designed using CMOS technology. It provides 500mA output current capability. The operating input voltage range is from 2.7V to 20V. The adjustable output voltage range is from 1.2V to ( $V_{IN} - V_{DROP}$ ).

Other features include logic-controlled shutdown mode, short-circuit current limit and thermal shutdown protection. The SLD609S has automatic discharge function to quickly discharge  $V_{OUT}$  in the disabled status.

The SLD609S is available in Green SOT23-5 packages. It operates over an operating temperature range of -40°C to +125°C.

## Features

- Input voltage range: 2.7V ~ 20V
- Fixed VOUT: 1.2V/1.5V/1.8V/2.5V/2.8V/3V/3.3V/3.8V/4.2V and 5.0V in different version
- Adjustable Output from 1.2V to ( $V_{IN} - V_{DROP}$ )
- Output accuracy:  $\pm 1\%$  for all version and temperature range
- High PSRR: 100 dB (TYP) @ 1KHz
- Low noise: 14 $\mu$ V<sub>RMS</sub> (TYP) @ 10Hz~100KHz
- Low Quiescent current: 39 $\mu$ A (TYP)
- Shutdown Supply Current: 1.2 $\mu$ A (TYP)
- Over Current protection
- Output Discharge
- Thermal Shutdown
- -40°C to +125°C Operating Temperature Range
- Excellent Load and Line Transient Responses
- Robust ESD immunity capability  
HBM >  $\pm 2$ KV  
CDM >  $\pm 1$ KV
- Available in Green SOT23-5 Packages

## Applications

- Instrumentation
- Precision ADC and DAC
- Precision Amplifiers in Industrial Equipment
- Low Noise VCO
- RF System
- Medical Equipment

### Typical Application

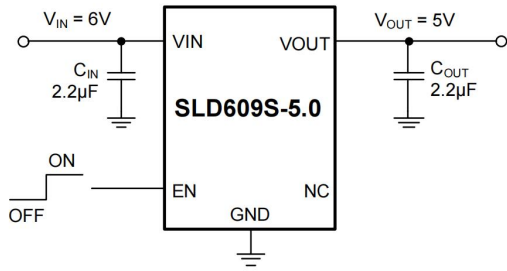


Figure 1. SLD609S with Fixed Output Voltage, 5V (SOT23-5)

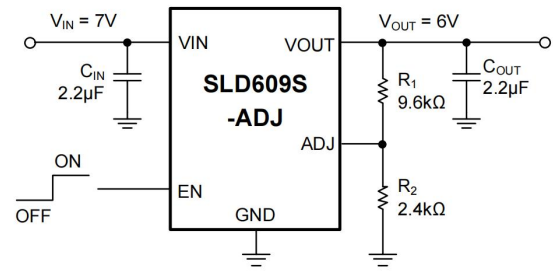


Figure 2. SLD609S with 1.2V Output Adjusted to 6V (SOT23-5)

### Block Diagram

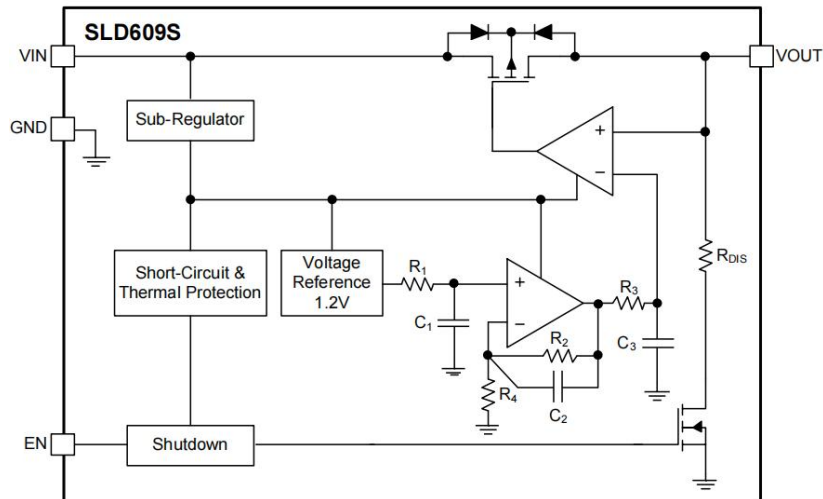
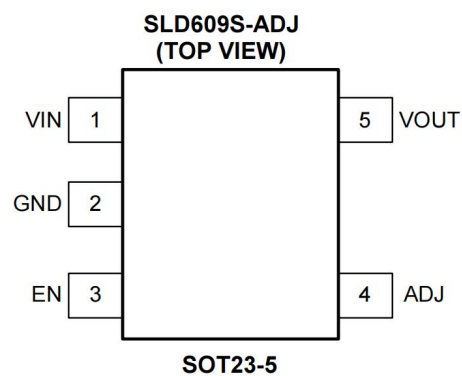
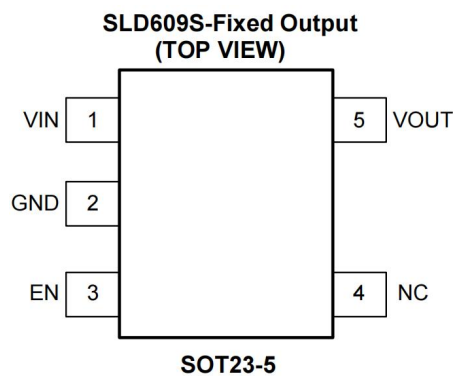


Figure 3. Block Diagram (SOT23-5 Fixed Version)

### Pin Configurations





## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V <sub>IN</sub>	IN to GND		-0.3	24	V
V <sub>OUT</sub>	OUT to GND		-0.3	24	V
V <sub>EN</sub>	EN to GND		-0.3	24	V
I <sub>IN</sub>	Input Current (Continuous)			1	A
I <sub>OUT</sub>	Output Current			1	A
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
T <sub>J</sub>	Maximum Junction Temperature			+150	°C
ESD	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	2		KV
	Charged Device Model, JESD22-C101	All Pins	1		

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance.

Parameters	Min.	Max.	Unit
Input Voltage: V <sub>IN</sub>	2.7	20	V
Operating Junction Temperature Range	-40	125	°C

**Electrical Characteristics**

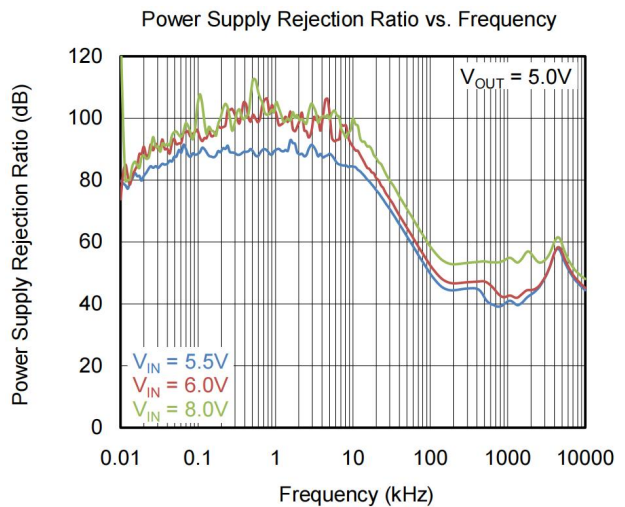
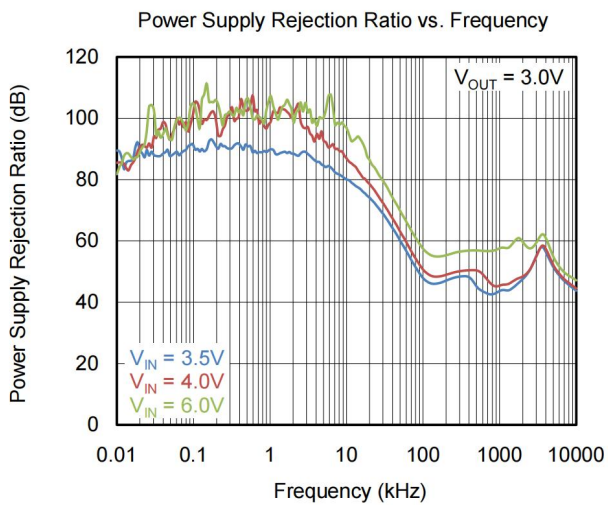
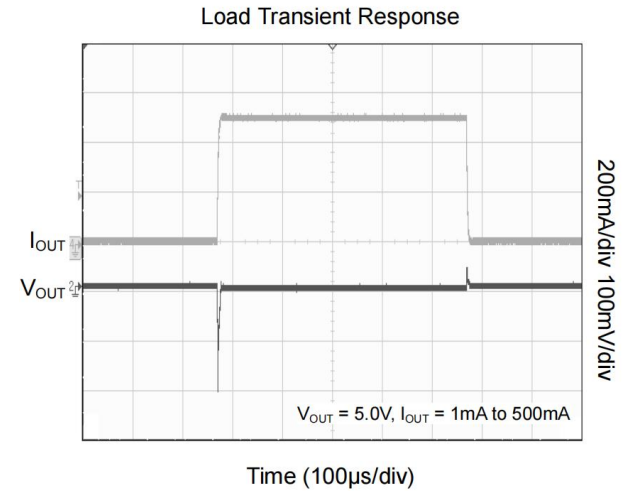
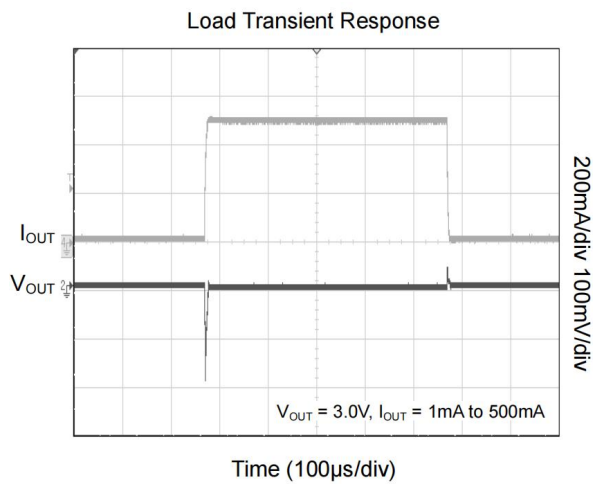
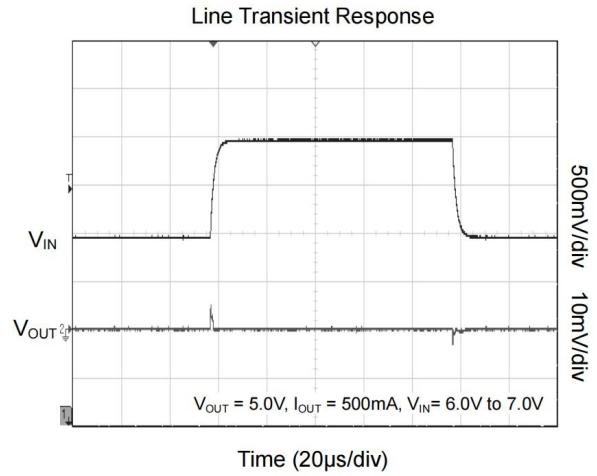
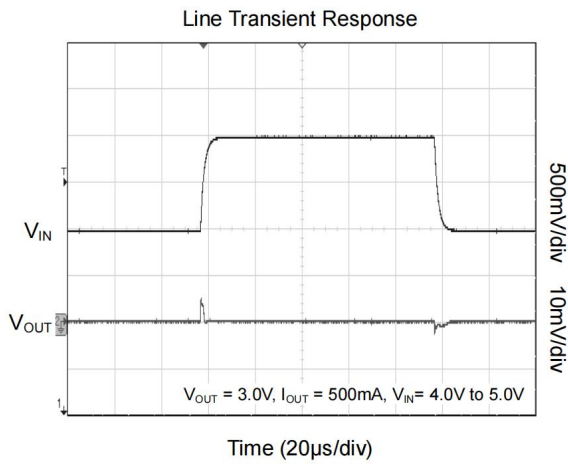
( $V_{IN} = (V_{OUT(NOM)} + 1V)$  or 2.7V (whichever is greater),  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 10mA$ ,  $C_{IN} = C_{OUT} = 2.2\mu F$  and  $C_{SS} = 0nF$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values are at  $T_J = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	$V_{IN}$		2.7		20	V
Under-Voltage Lockout Thresholds	$V_{UVLO}$	$V_{IN}$ rising		2.52	2.70	V
		$V_{IN}$ falling	2.16	2.33		
Operating Supply Current	$I_{GND}$	$I_{OUT} = 0\mu A$		39	62	$\mu A$
		$I_{OUT} = 500mA$		980	1200	
Shutdown Current	$I_{SHDN}$	$V_{EN} = GND$		1.2	2.2	$\mu A$
		$V_{EN} = GND$ , $V_{IN} = 20V$		1.3	2.5	
ADJ Input Bias Current	$I_{ADJ}$	$V_{ADJ} = V_{OUT(NOM)} + 0.1V$	-6		6	nA
Output Voltage Accuracy	$V_{OUT}$	$V_{IN} = (V_{OUT(NOM)} + 1V)$ to 20V, $I_{OUT} = 100\mu A$ to 500mA, $T_J = +25^{\circ}C$	-1		1	%
		$V_{IN} = (V_{OUT(NOM)} + 1V)$ to 20V, $I_{OUT} = 100\mu A$ to 500mA, $T_J = -40^{\circ}C$ to $+125^{\circ}C$	-1.6		1.6	
Feedback Voltage	$V_{ADJ}$	$I_{OUT} = 10mA$ , $T_J = +25^{\circ}C$	1.188	1.2	1.212	V
		$V_{IN} = (V_{OUT(NOM)} + 1V)$ to 20V, $I_{OUT} = 100\mu A$ to 500mA, $T_J = -40^{\circ}C$ to $+125^{\circ}C$	1.181		1.219	
Input Reverse Current	$I_{REV-INPUT}$	$V_{EN} = GND$ , $V_{IN} = 0V$ , $V_{OUT} = 20V$		0.05	1	$\mu A$
Line Regulation	$\Delta V_{OUT}$	$V_{IN} = (V_{OUT(NOM)} + 1V)$ to 20V		0.001	0.007	%/V
	$\Delta V_{IN} \times V_{OUT}$					
Load Regulation	$\Delta V_{OUT}$	$I_{OUT} = 100\mu A$ to 500mA		3	26	mV
Dropout Voltage <sup>(1)</sup>	$V_{DROP}$	$I_{OUT} = 500mA$	$V_{OUT(NOM)} = 2.5V$	500	730	mV
			$V_{OUT(NOM)} = 3.0V$	450	680	
			$V_{OUT(NOM)} = 5.0V$	360	580	
Soft-Start Source Current	$SS_{I-SOURCE}$	$SS = GND$		1	3	$\mu A$
Output Current Limit	$I_{LIMIT}$	$V_{OUT} = V_{OUT(NOM)} - 1V$ (2)	0.51	0.80		A
Output Voltage Noise	$e_n$	$f = 10Hz$ to $100kHz$ , $I_{OUT} = 1mA$	$V_{OUT} = 1.2V$	9.3		$\mu VRMS$
			$V_{OUT} = 2.8V$	11		
			$V_{OUT} = 5.0V$	14		
Power Supply Rejection Ratio	PSRR	$V_{IN} = V_{OUT(NOM)} + 1V$	$f = 1kHz$	100		dB
			$f = 10kHz$	83		
			$f = 100kHz$	52		
			$f = 1MHz$	55		
Precision EN Input	$V_{IH}$	Logic high, $V_{IN} = 2.7V$ to 20V	1.120	1.210	1.295	V
	$V_{IL}$	Logic low, $V_{IN} = 2.7V$ to 20V	1.050	1.120	1.195	
Leakage Current	$I_{EN-LKG}$	$V_{EN} = V_{IN}$ , $V_{IN} = 2.7V$ to 20V		0.1	1	$\mu A$
Start-Up Time	$t_{STR}$	From EN rising from 0V to $V_{IN}$ to $0.9 \times V_{OUT}$ , $V_{OUT} = 1.2V$		150		$\mu s$
Output Discharge Resistance	$R_{DIS}$	$V_{EN} = 0V$ , $V_{OUT} = 0.5V$		100	140	$\Omega$
Thermal Shutdown Temperature	$T_{SHDN}$			160		$^{\circ}C$
Thermal Shutdown Hysteresis	$\Delta T_{SHDN}$			20		$^{\circ}C$

**NOTES:**

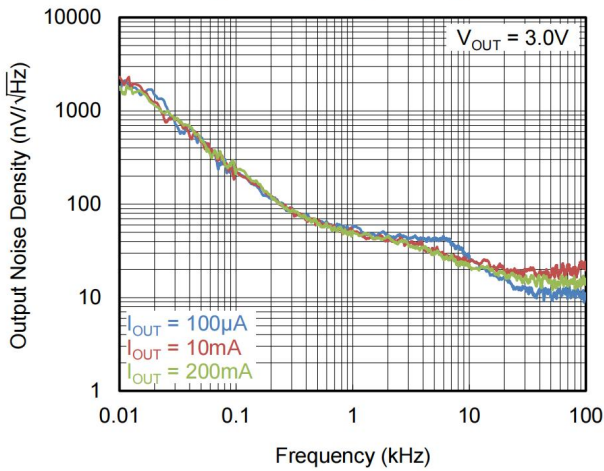
- The dropout voltage is defined as the difference between  $V_{IN}$  and  $V_{OUT}$  when  $V_{OUT}$  falls to  $95\% \times V_{OUT(NOM)}$ .
- $V_{OUT} = V_{OUT(NOM)} - 0.2V$  when  $V_{OUT} = 1.2V$ .

## Typical Characteristics

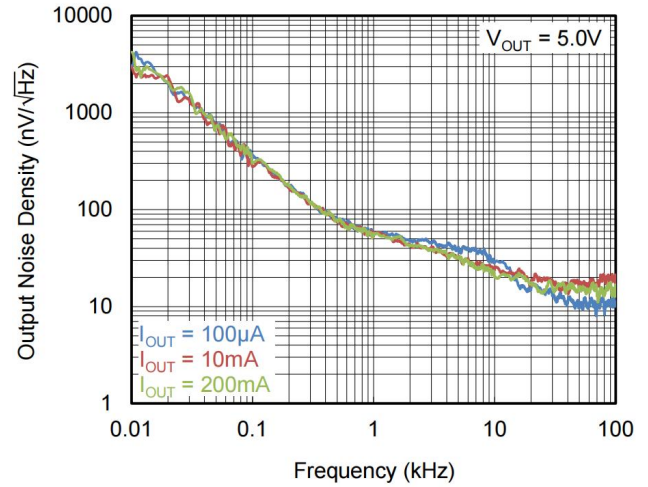


**Typical Characteristics(continued)**

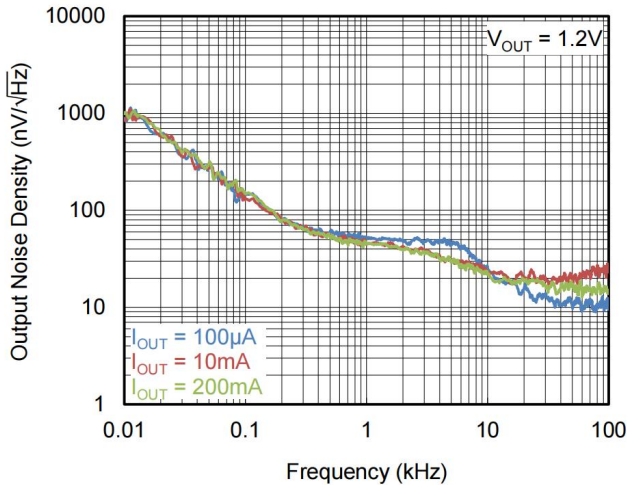
Output Noise Density vs. Frequency



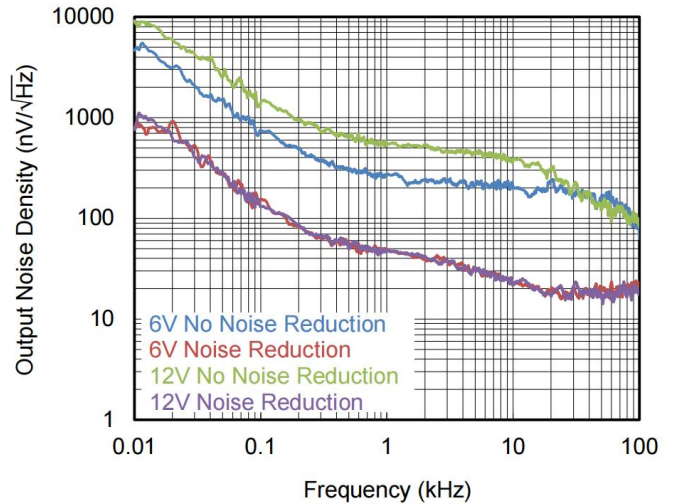
Output Noise Density vs. Frequency



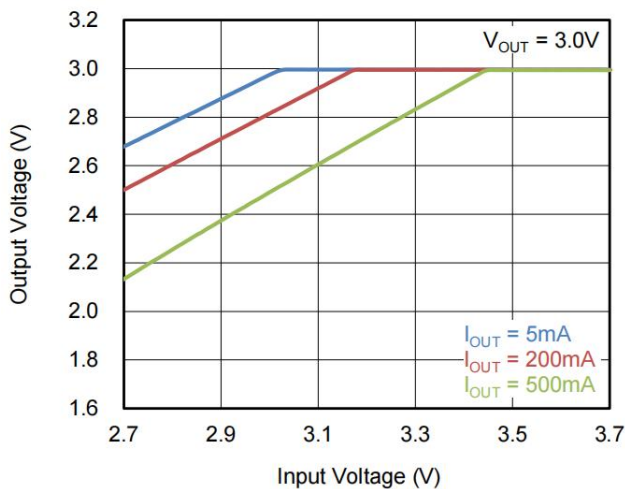
Output Noise Density vs. Frequency



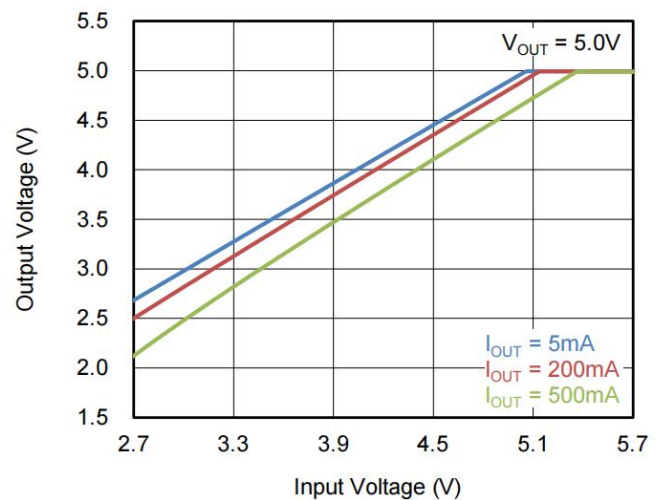
Output Voltage with/without Noise Reduction

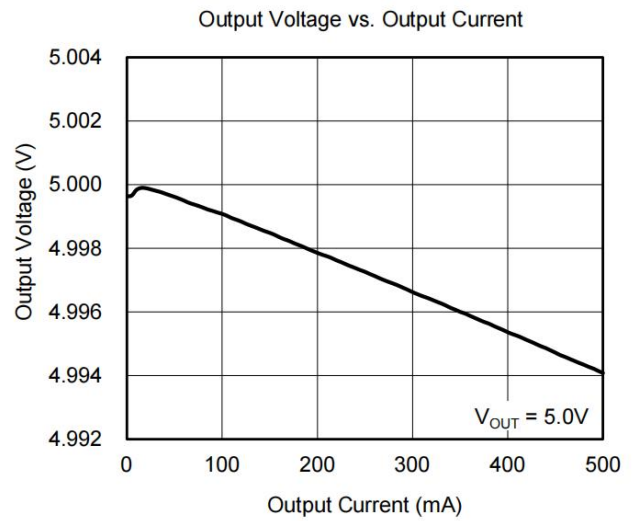
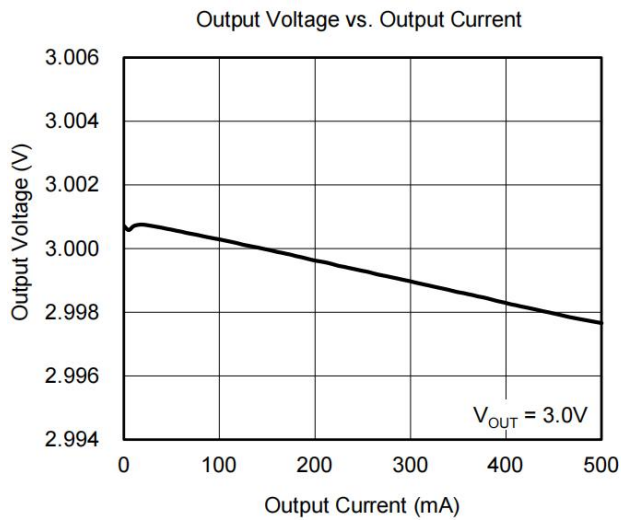
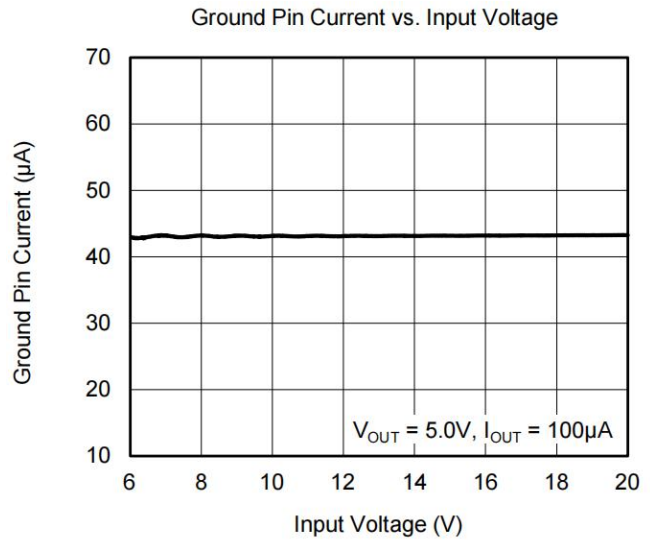
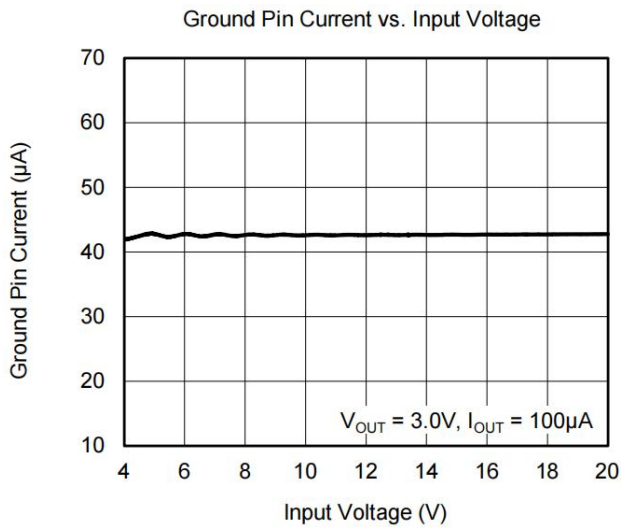
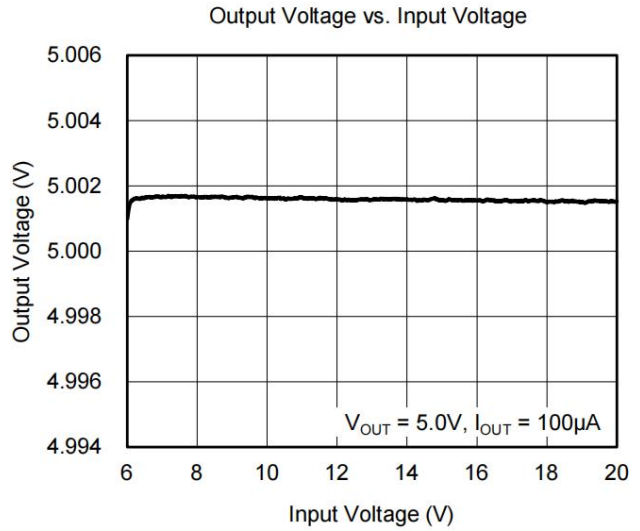
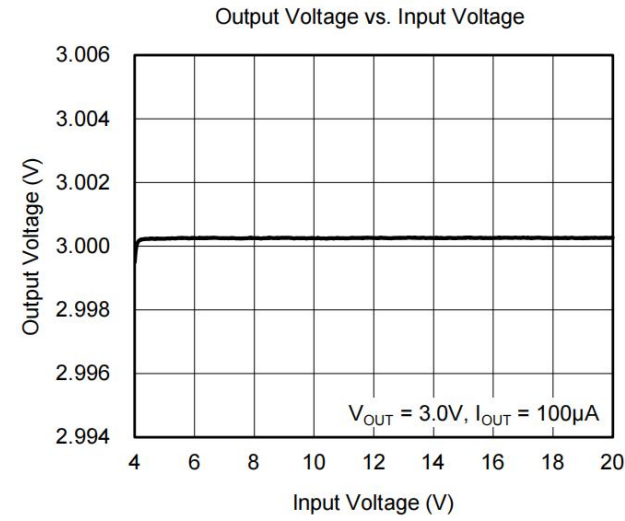


Output Voltage vs. Input Voltage in Dropout

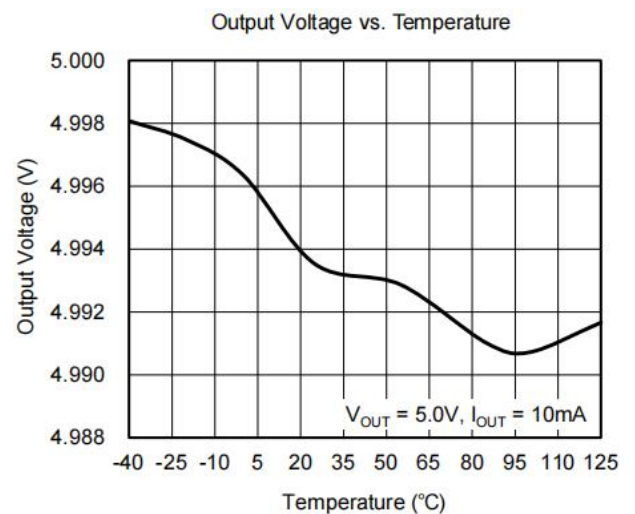
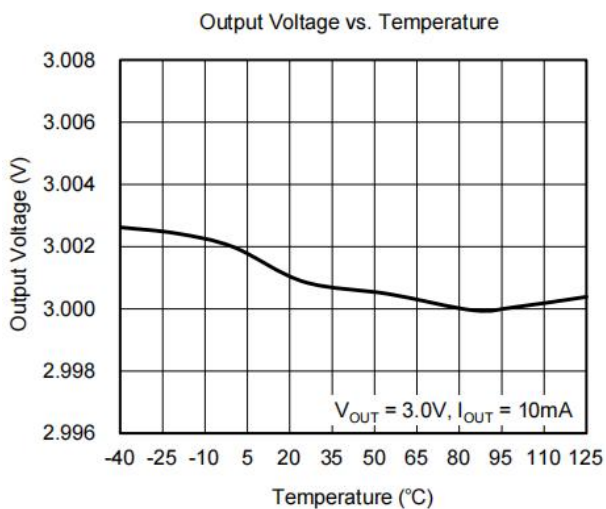
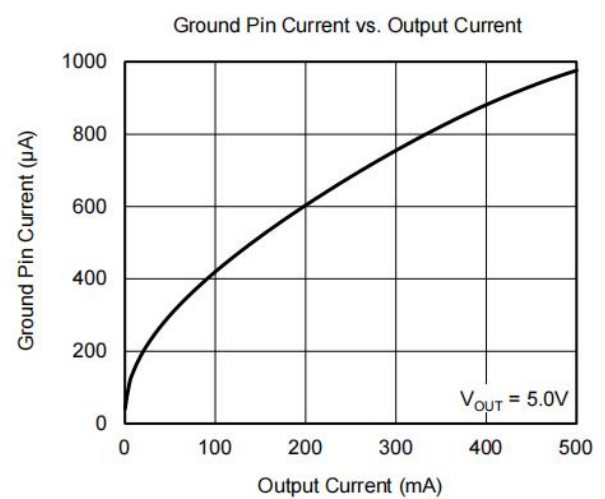
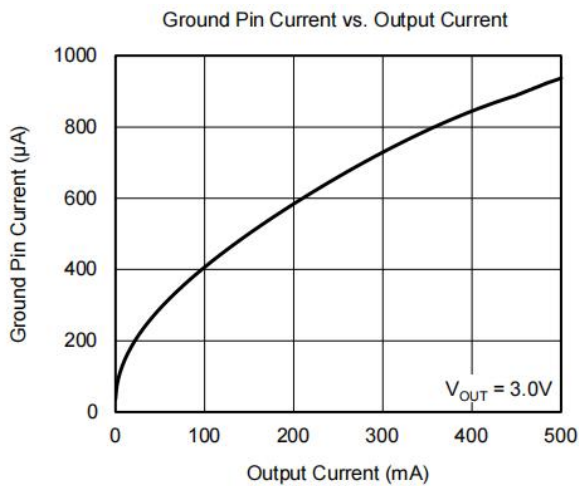
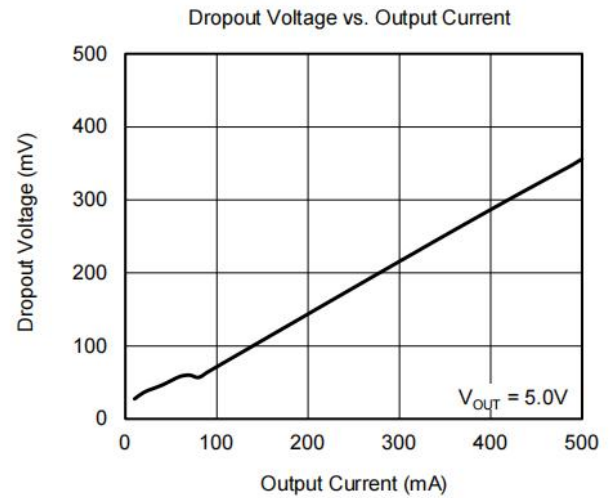
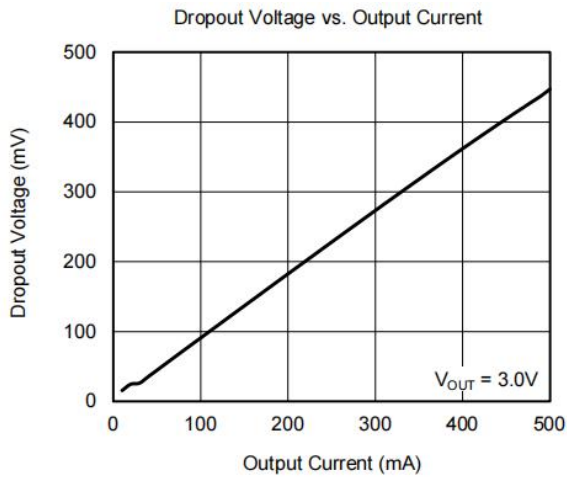


Output Voltage vs. Input Voltage in Dropout

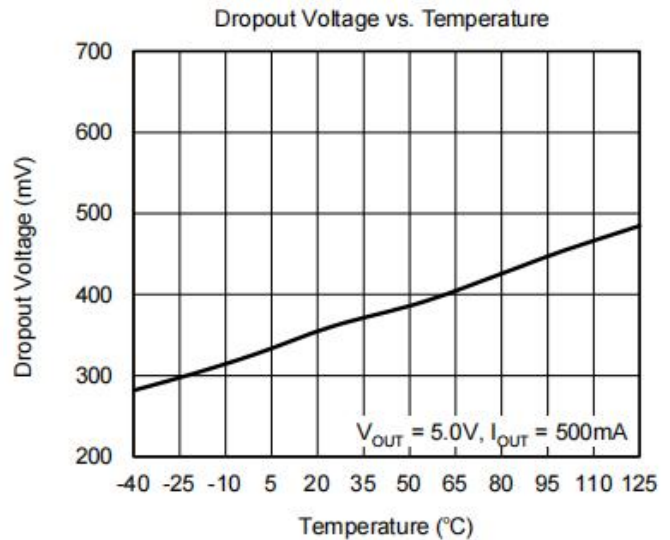
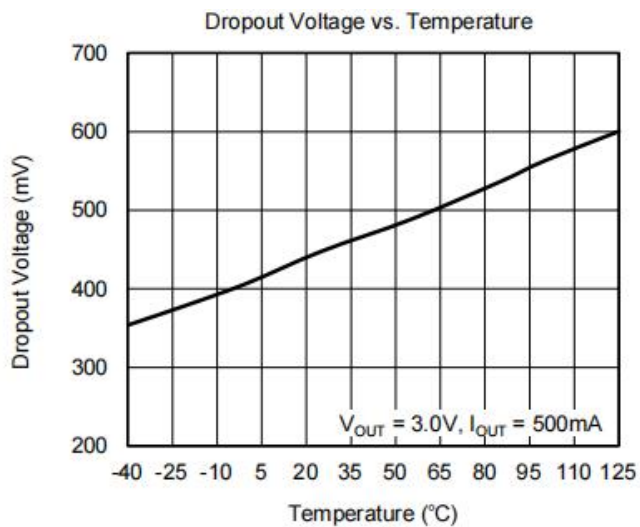
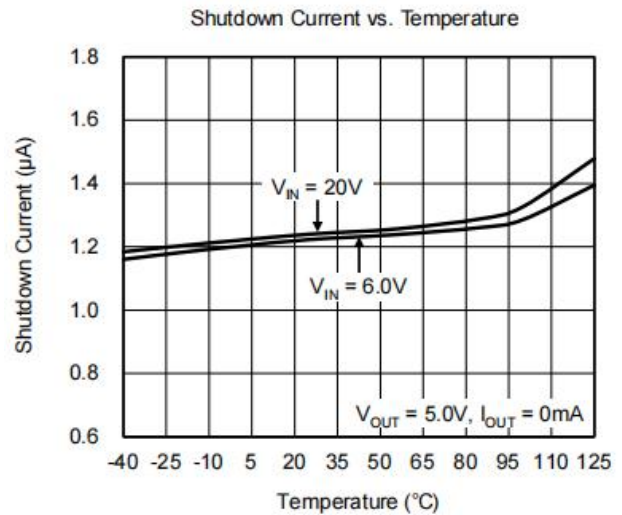
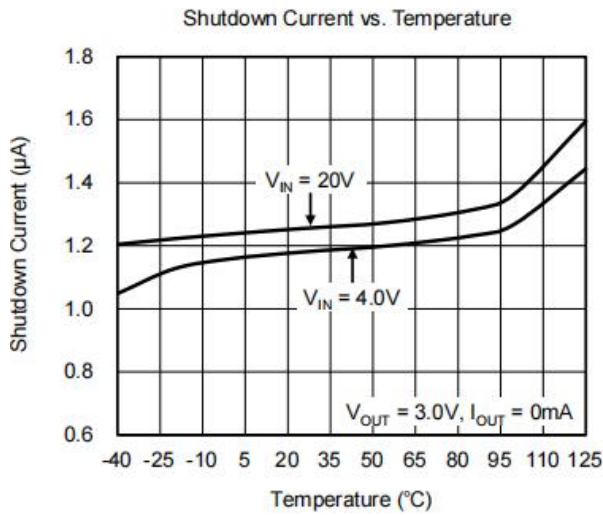
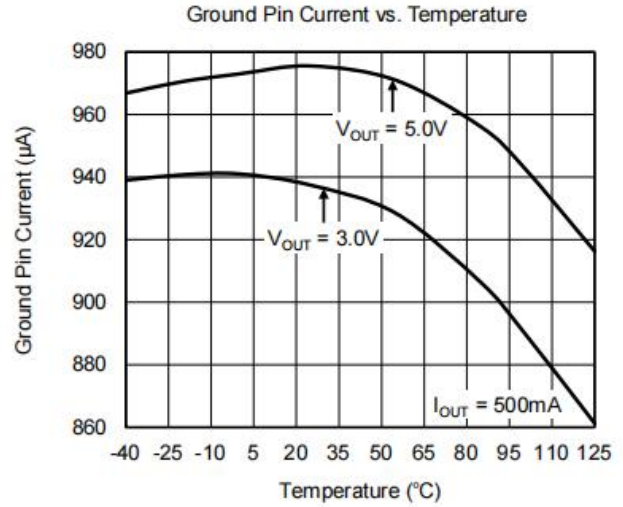
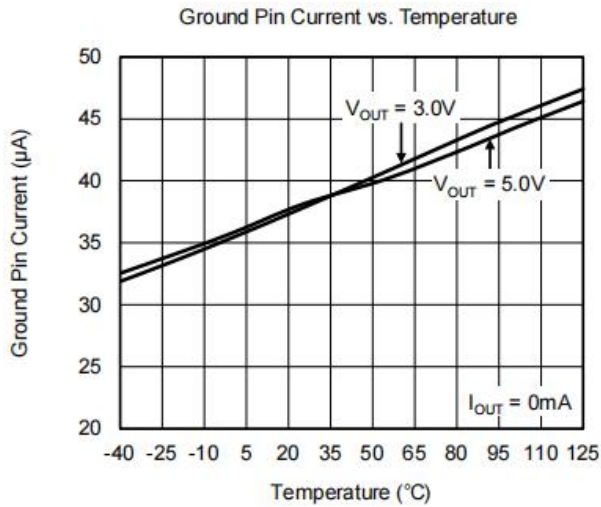


**Typical Characteristics(continued)**




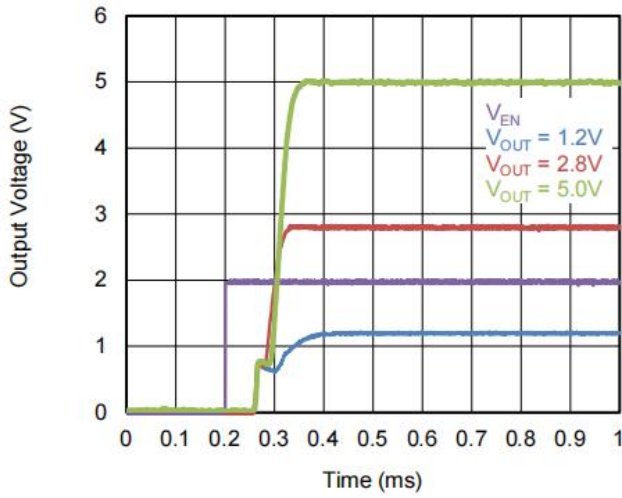
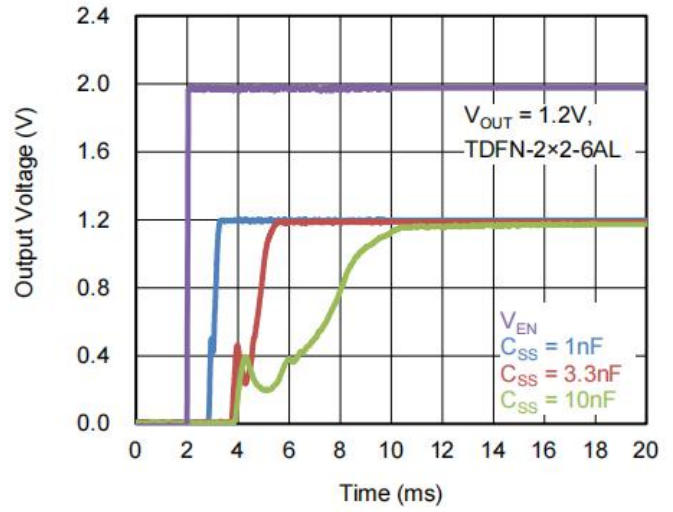
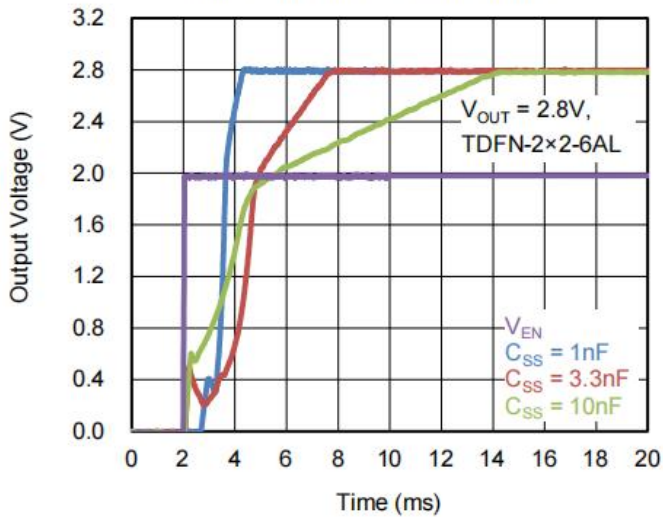
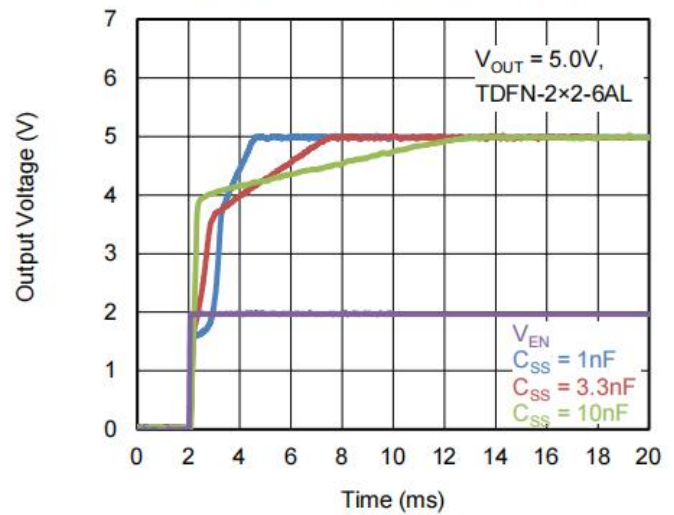
**Typical Characteristics(continued)**




**Typical Characteristics(continued)**


**Typical Characteristics(continued)**

Typical Start-Up Behavior


 Typical Soft-Start Behavior, Different C<sub>SS</sub>

 Typical Soft-Start Behavior, Different C<sub>SS</sub>

 Typical Soft-Start Behavior, Different C<sub>SS</sub>


## APPLICATION INFORMATION

The SLD609S is a low noise, fast transient response high performance LDO, it consumes only 39 $\mu$ A (TYP) quiescent current and provides 500mA output current. The SLD609S provides the protection function for output overload, output short-circuit condition and overheating.

### Input Capacitor ( $C_{IN}$ )

The input decoupling capacitor should be placed as close as possible to the  $V_{IN}$  pin to ensure the device stability. 2.2 $\mu$ F or greater X7R or X5R ceramic capacitor is selected to get good dynamic performance.

When  $V_{IN}$  is required to provide large current instantaneously, a large effective input capacitor is required. Multiple input capacitors can limit the input tracking inductance. Adding more input capacitors is available to restrict the ringing and to keep it below the device absolute maximum ratings.

### Output Capacitor ( $C_{OUT}$ )

The output capacitor should be placed as close as possible to the  $V_{OUT}$  pin. A 2.2 $\mu$ F or greater X7R or X5R ceramic capacitor is selected to get good dynamic performance. The minimum effective capacitance of  $C_{OUT}$  that SLD609S can remain stable is 2.2 $\mu$ F. For ceramic capacitor, temperature, DC bias and package size will change the effective capacitance, so enough margin of  $C_{OUT}$  must be considered in design. Additionally,  $C_{OUT}$  with larger capacitance and lower ESR will help increase the high frequency PSRR and improve the load transient response.

## Programmable Precision Enable Operation

The SLD609S uses the EN pin to enable/disable the device and to deactivate/activate the output automatic discharge function.

When the EN pin voltage is lower than 1.1V, the device is in shutdown state. There is no current flowing from  $V_{IN}$  to  $V_{OUT}$  pins. In this state, the automatic discharge transistor is active to discharge the output voltage through a 100 $\Omega$  (TYP) resistor.

When the EN pin voltage is higher than 1.2V, the device is in active state. The output voltage is regulated to the expected value and the automatic discharge transistor is turned off.

The EN pin voltage threshold can be programmed by the user and set above the nominal 1.2V by using two resistors ( $R_{EN1}$ ,  $R_{EN2}$ ) as shown in Figure 7. The nominal range of  $R_{EN2}$  is 10K $\Omega$  to 100k $\Omega$  and the resistance value of  $R_{EN1}$  can be determined by the following equation:

$$R_{EN1} = R_{EN2} \times (V_{IN} - 1.2V) / 1.2V \quad (1)$$

where  $V_{IN}$  is the required starting voltage.

The coefficient of hysteresis voltage increase can be calculated through  $(R_{EN1} + R_{EN2}) / R_{EN2}$ . It is calculated that the EN pin voltage threshold is 3.6V and the voltage increase is 300mV.

## Soft-Start

When the device is enabled, the SLD609S has an internal soft-start (SS pin open) to limit the inrush current. When  $V_{OUT} = 1.2V$ , the start-up time is  $150\mu s$  (TYP).

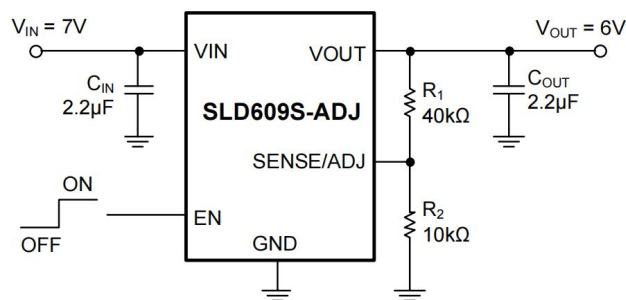
## Adjustable Regulator

The output voltage of the SLD609S-1.2 can be adjusted from 1.2V to  $(V_{IN} - V_{DROP})$ . The ADJ pin will be connected with two external resistors as shown in Figure 4, the output voltage is determined by the following equation:

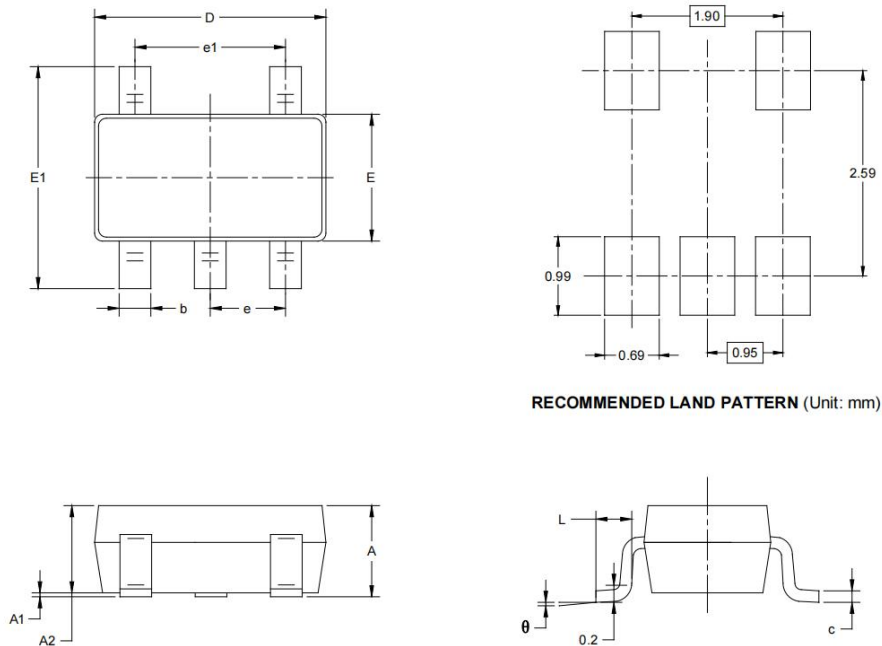
$$V_{OUT} = V_{ADJ} \times \left( 1 + \frac{R_1}{R_2} \right) \quad (2)$$

where:

$V_{OUT}$  is output voltage and  $V_{ADJ}$  is the internal voltage reference,  $V_{ADJ} = 1.2V$ . The parallel capacitor ( $C_{FF}$ ) with  $R_1$  can be used to improve the feedback loop stability and PSRR, increase the transient response and reduce the AC gain of the error amplifier and output noise.



**Figure 4. SLD609S with 1.2V Output Adjusted to 6V**

**PACKAGE SOT23-5**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

**NOTES:**

1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

**PACKAGE/ORDERING INFORMATION**

Product Name	①②③④⑤	Set Voltage	Package	Units Reel
SLD609S121A	C11XX	1.2V	SOT23-5	3000
SLD609S151A	C12XX	1.5V	SOT23-5	3000
SLD609S181A	C13XX	1.8V	SOT23-5	3000
SLD609S251A	C14XX	2.5V	SOT23-5	3000
SLD609S281A	C15XX	2.8V	SOT23-5	3000
SLD609S301A	C16XX	3.0V	SOT23-5	3000
SLD609S331A	C17XX	3.3V	SOT23-5	3000
SLD609S381A	C18XX	3.8V	SOT23-5	3000
SLD609S421A	C19XX	4.2V	SOT23-5	3000
SLD609S501A	C1AXX	5.0V	SOT23-5	3000
SLD609S-ADJ	C2FXX	1.2V to ( $V_{IN} - V_{DROP}$ )	SOT23-5	3000



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