General Description

The SGD824x isolated driver family is an isolated dual channel gate driver with different configurations. The SGD8243/4 are configured as high-side/low-side drivers, while the SGD8245 are configured as dual drivers. The peak source output current is 4.0A and the peak sink output current is 6.0A. Programmable dead time (DT) feature is available in SGD8243/4. Pulling high the DIS pin shuts down both outputs simultaneously, and allows for normal operation when the DIS pin is open or pulled low. As a fail-safe measure, primary-side logic failures force both outputs low. The VDDA and VDDB supply voltage are up to 25 V. A wide input VDDI range from 3 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have under voltage lock-out (UVLO) protection. The SGD824x has 5.0kVRMS isolation in SOP16W package and 3.0kVRMS isolation in SOP16 package per UL1577. High CMTI, low propagation delay, small size and flexible configuration make the SGD824x family is suitable for a wide range of isolated MOSFET/IGBT and SiC or GaN FET gate drive applications.

Features

- 4.0A peak source current & 6.0A peak sink current
- 40ns (Typ.) propagation delay
- 10ns (Max.) pulse width distortion & 10ns (Max.) channel delay matching
- 100kV/us (Min.) common mode transient immunity (CMTI)
- Wide input voltage: 3V to 18V
- Up to 25V driver output voltage
- 5V reverse polarity voltage handling capability on input stage
- Operating temperature: –40°C to +125°C
- Safety certifications (Pending):
  - 5kVRMS isolation for 1 minute per UL 1577 with SOP16W, SOP14W package
  - 3kVRMS isolation for 1 minute per UL 1577with SOP16 package
  - DIN V VDE 0884-11

Package Marking and Ordering Information

Part Number	Marking	Package	Units/Tube	Units/Reel
SGD824x	SGD824x	SOP14W/16W		1500
SGD824x	SGD824x	SOP16		3000

Applications

- AC/DC or DC/DC power supplies in server, telecom and industry
- DC/AC solar inverters
- EV battery charging

APPLICATION CIRCUIT

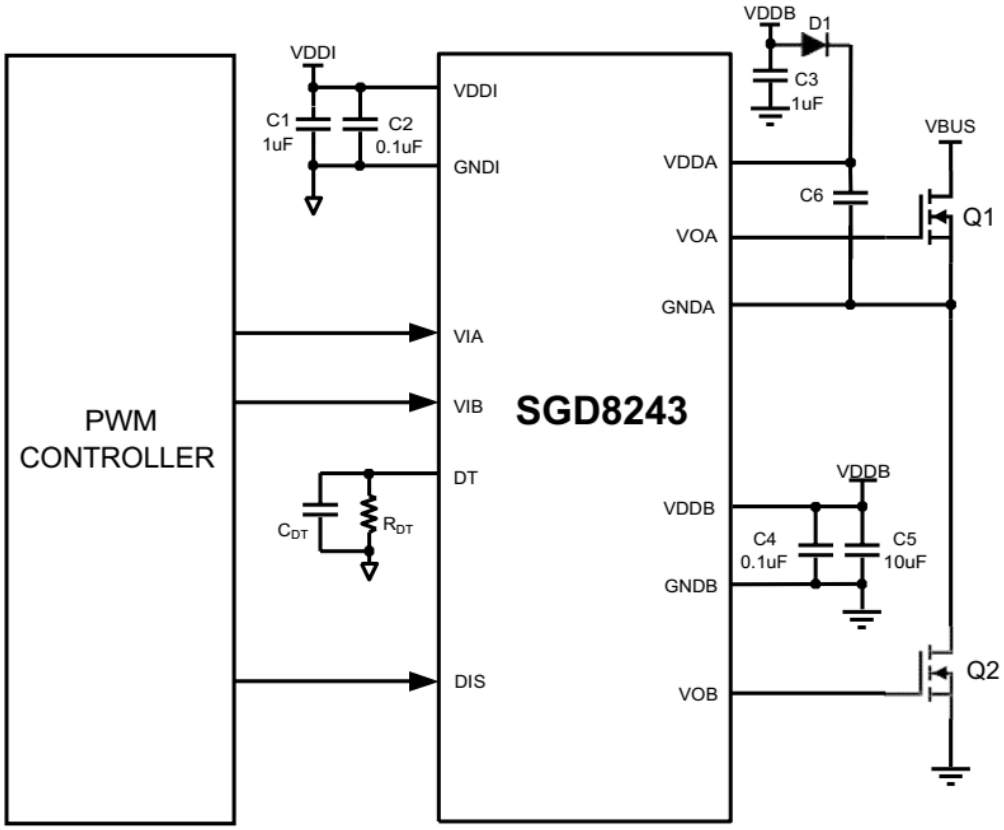


Figure 1. SGD8243 Application Circuit

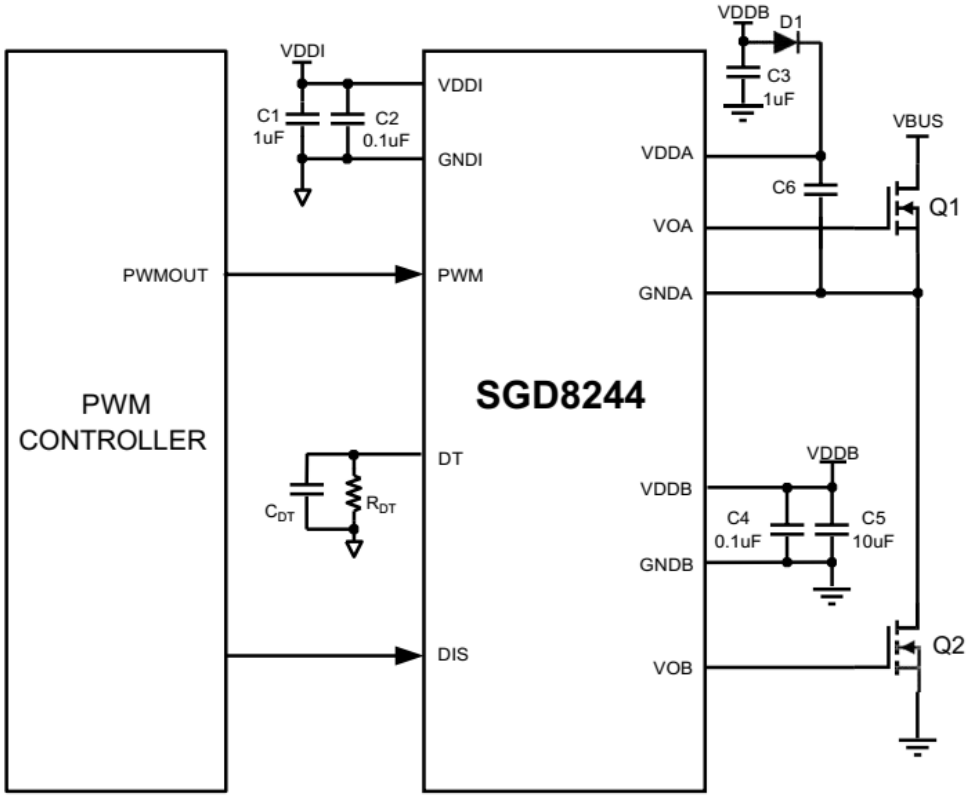


Figure 2. SGD8244 Application Circuit

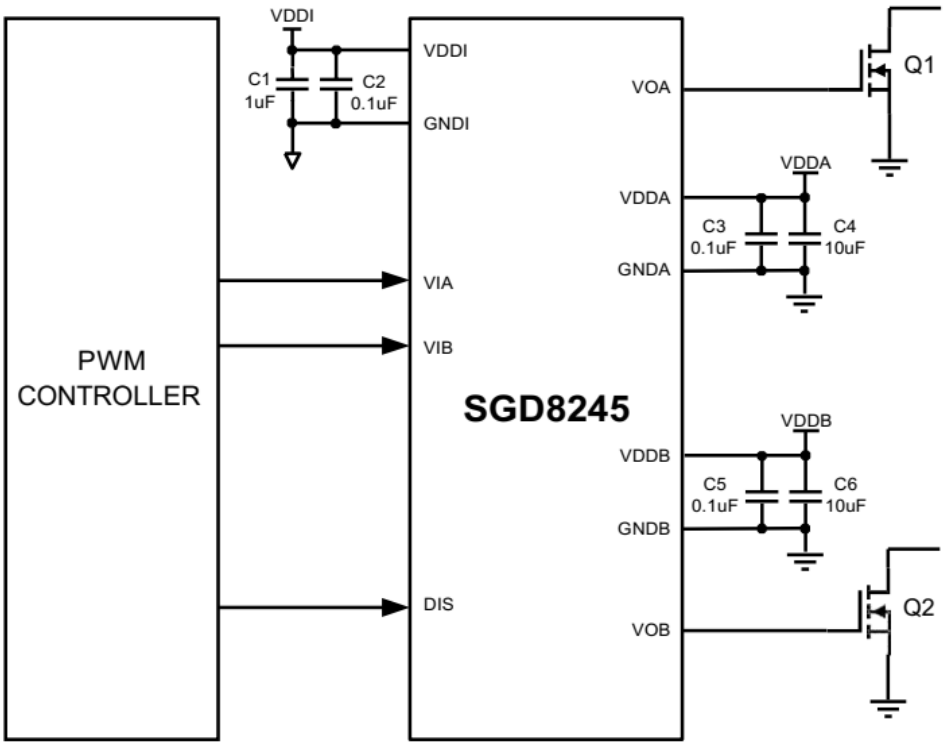
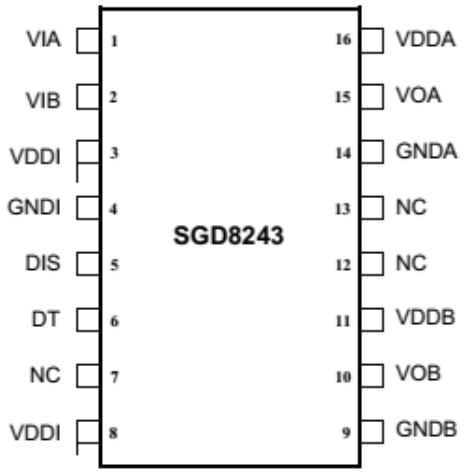
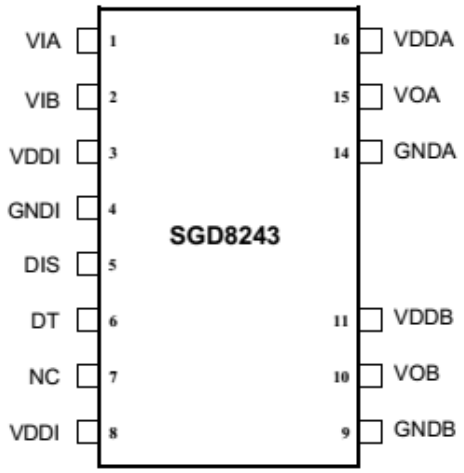
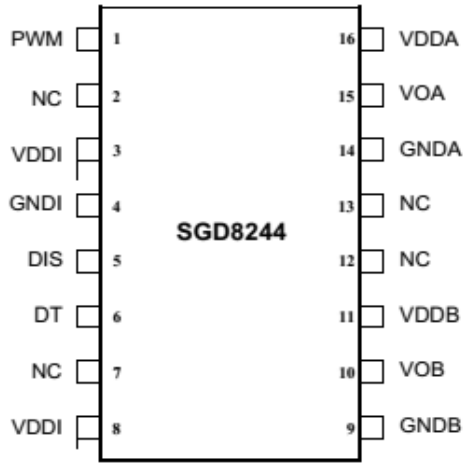
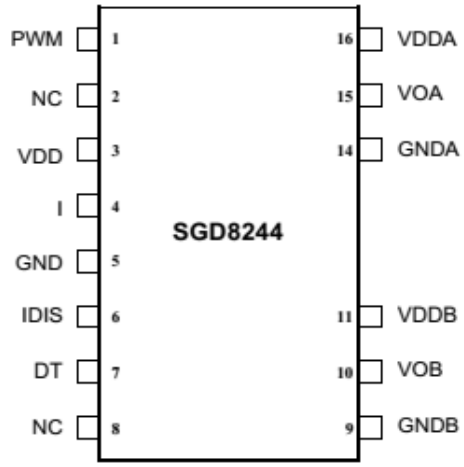
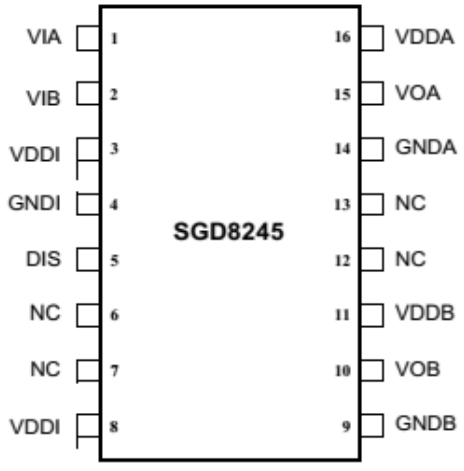
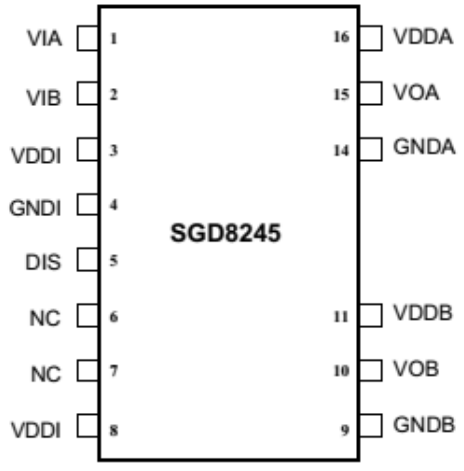


Figure 3. SGD8245 Application Circuit

PIN CONFIGURATION

Part Number	Pin Configuration (Top View)	
	SOP16/ SOP16W	SOP14W
SGD8243		
SGD8244		
SGD8245		

PIN DESCRIPTION

Table 1. SGD8243 Pin Description

No.	Pin	Description
1	VIA	Input of driver A. The output of driver A is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
2	VIB	Input of driver B. The output of driver B is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	DIS	Device disable input. When DIS pin is high, both driver is disabled and driver outputis low. When DIS pin is low, it allows the device to perform in normal operation.
6	DT	Dead time programming input. Connect a resistor between DT and GNDI to program the dead time. A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.
7	NC	No connection
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDB and GNDB.
12	NC	No connection. Pin12 is removed in SOP14W
13	NC	No connection. Pin13 is removed in SOP14W
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

Table 2. SGD8244 Pin Description

No.	Pin	Description
1	PWM	PWM input. The output of driver A is in phase with PWM input and the output of driver B is out of phase with PWM input.
2	NC	No connection
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	DIS	Device disable input. When DIS pin is high, both driver is disabled and driver output is low. When DIS pin is low, it allows the device to perform in normal operation.
6	DT	Dead time programming input. Connect a resistor between DT and GNDI to program the dead time. A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.
7	NC	No connection
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDB and GNDB.
12	NC	No connection. Pin12 is removed in SOP14W
13	NC	No connection. Pin13 is removed in SOP14W
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

Table 3. SGD8245 Pin Description

No.	Pin	Description
1	VIA	Input of driver A. The output of driver A is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
2	VIB	Input of driver B. The output of driver B is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	DIS	Device disable input. When DIS pin is high, both driver is disabled and driver outputis low. When DIS pin is low, it allows the device to perform in normal operation.
6	NC	No connection
7	NC	No connection
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDB and GNDB.
12	NC	No connection. Pin12 is removed in SOP14W
13	NC	No connection. Pin13 is removed in SOP14W
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

FUNCTIONAL BLOCK DIAGRAM

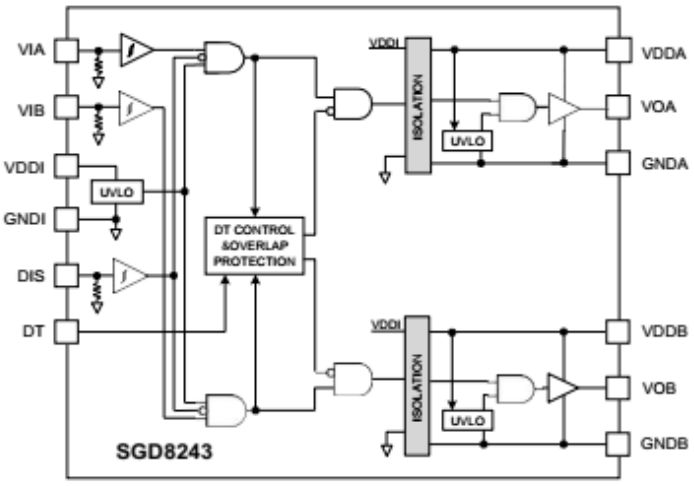


Figure 4. SGD8243 Functional Block Diagram

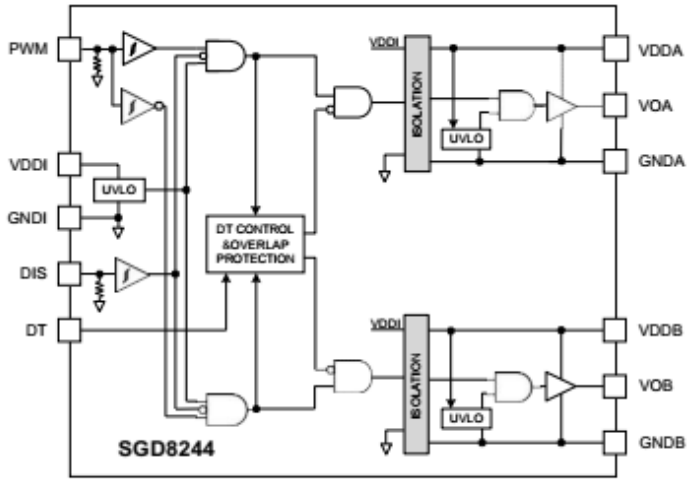


Figure 5. SGD8244 Functional Block Diagram

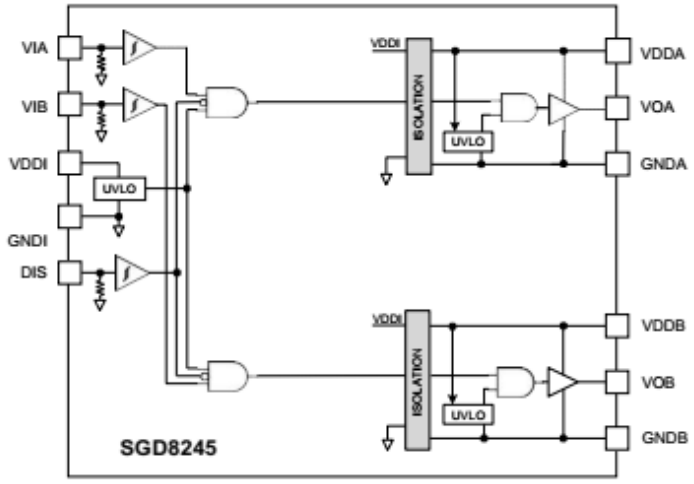


Figure 6. SGD8245 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Definition		Min	Max	Unit
V_{DDI}	Input Power Supply Voltage		-0.5	20	V
V_{IA},V_{IB}, V_{DIS},V_{PWM}	Input Signal Voltage		-7	20	V
V_{DDA}, V_{DDB}	Driver Power Supply		-0.5	30	V
V_{OUTA}, V_{OUTB}	Driver Output Voltage		-0.5	30	V
V_{ch2ch}	Channel to Channel Voltage, GNDA to GNDB	SOP16W/SOP16		1500	V
		SOP14W		1850	V
T_J	Junction Temperature		-40	150	°C
T_S	Storage Temperature		-65	150	°C

RECOMMENDED OPERATION CONDITIONS[1]

Symbol	Definition	Min	Max	Unit
V_{DDI}	Input Power Supply Voltage	3	18	V
V_{IA},V_{IB}, V_{DIS},V_{PWM}	Input Signal Voltage	-5	18	V
V_{DDA}, V_{DDB}	Driver Power Supply for 3.5V UVLO	4	25	V
V_{DDA}, V_{DDB}	Driver Power Supply for 5.5V UVLO	6	25	V
V_{DDA}, V_{DDB}	Driver Power Supply for 8.5V UVLO	9	25	V
V_{DDA}, V_{DDB}	Driver Power Supply for 12.5V UVLO	13.5	25	V
T_J	Junction Temperature	-40	150	°C
T_A	Ambient Temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM	±4000	V
	CDM	±2000	

THERMAL INFORMATION

Symbol	Definition	Value		Unit
		SOP16W/SOP14W	SOP16	
$R_{\theta JA}$	Junction to ambient thermal resistance	100	TBD	°C/W
$R_{\theta JC(TOP)}$	Junction to case (top) thermal resistance	40	TBD	°C/W

Note 1: V_{DDI}, V_{IA}, V_{IB}, V_{DIS}, V_{PWM} are reference to GNDI; V_{DDA}, V_{OUTA} are referenced to GNDA; V_{DDB}, V_{OUTB} arereferenced to GNDB;

PACKAGE SPECIFICATIONS

Symbol	Definition	Min.	Typ.	Max.	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		1.8		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value		Units
			SOP16	SOP16W/ SOP14W	
CLR	External clearance	Shortest terminal to terminal distance through air	>4.0	>8.0	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	>4.0	>8.0	mm
DTI	Distance through the insulation	Minimum internal gap	>16	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	>600	V
	Material Group		I	I	
	Overvoltage category	Rated mains voltages ≤150Vrms	I-IV	I-IV	
		Rated mains voltages ≤300Vrms	I-III	I-IV	
		Rated mains voltages ≤600Vrms	I-II	I-III	
		Rated mains voltages ≤1000Vrms	I-I	I-II	

DIN V VDE 0884-11(1)					
V_{IORM}	Maximum repetitive peak isolation voltage		1000	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage		707	1060	V_{RMS}
V_{IOTM}	Maximum transient isolation voltage	60s	4242	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368-1, 1.2/50us waveform, V_{TEST}=1.6 x V_{IOSM} for SOP16W/SOP14W; V_{TEST}=1.3 x V_{IOSM} for SOP16	6000	6250	V_{PK}
q_{pd}	Apparent charge	Method b2: $V_{pd(m)}$=1.875 x V_{IORM} for SOP16W/SOP14W and $V_{pd(m)}$=1.5 x V_{IORM} for SOP16, tm=1 s	≤5	≤5	pC
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	
UL1577(1)					
V_{ISO}	Withstand Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	3000	5000	V_{RMS}

Note 1: Certification pending

ELECTRICAL CHARACTERISTICS (DC)

V_{DDI} = 5 V, 0.1μF capacitor from VDDI to GNDI, V_{DDA} = V_{DDB} =15V, 1μF capacitor from VDDA and VDDB to GNDAand GNDB, T_A = –40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input Power Supply						
V_{DDI}	Input Supply Voltage		3		18	V
$V_{UVLO\_VDDI\_R}$	VDDI UVLO Rising		2.55	2.7	2.85	V
$V_{UVLO\_VDDI\_F}$	VDDI UVLO Falling		2.35	2.5	2.65	V
V_{UVLO_HYS}	VDDI UVLO Hysteresis			0.2		V
I_{VDDI}	Quiescent Current	V_{IA} = 0V, V_{IB} = 0V		2		mA
	Operation Current	C_{LOAD}=100pF, f_{sw}= 50kHz, (50% Duty Cycle), each channel		2.5		mA

Logic Interface						
V_{IH}	High Level Input Threshold Voltage at VIA, VIB, DIS and PWM		2			V
V_{IL}	Low Level Input Threshold Voltage at VIA, VIB, DIS and PWM				0.8	V
R_{PD}	Pull down Resistance on VIA,VIB,DIS and PWM			200		kΩ
Driver Power Supply						
$V_{UVLO\_VDDA\_R}$, $V_{UVLO\_VDDB\_R}$	VDDA, VDDB UVLO Rising	3.5V UVLO Version	3.2	3.5	3.8	V
		5.5V UVLO Version	5.1	5.5	5.9	V
		8.5V UVLO Version	8	8.5	9	V
		12.5V UVLO Version	11.5	12.5	13.5	V
$V_{UVLO\_VDDA\_F}$, $V_{UVLO\_VDDB\_F}$	VDDA, VDDB UVLO Falling	3.5V UVLO Version	2.7	3	3.3	V
		5.5V UVLO Version	4.6	5	5.4	V
		8.5V UVLO Version	7	7.5	8	V
		12.5V UVLO Version	10.5	11.5	12.5	V
$V_{UVLO\_VDDA\_HYS}$, $V_{UVLO\_VDDB\_HYS}$	VDDA, VDDB UVLO Hysteresis	3.5V UVLO Version		0.5		V
		5.5V UVLO Version		0.5		V
		8.5V UVLO Version		1		V
		12.5V UVLO Version		1		V
I_{VDDA}, I_{VDDB}	Quiescent Current	V_{IA} = 0V, V_{IB} = 0V		1.2		mA
	Operation Current	C_{LOAD}=100pF, f_{sw}= 50kHz, (50% Duty Cycle), each channel		2		mA

OUTPUT

I_{OH}	Peak Source Current			4		A
I_{OL}	Peak Sink Current			6		A
V_{OH}	High Level Output Voltage	I_O=-10mA		25	50	mV
V_{OL}	Low Level Output Voltage	I_O=10mA		15	30	mV

Dead Time

R_{DT}	Resistance range on DT		5		220	kΩ
t_{DT}	Dead time	R_{DT}=20kΩ	160	200	240	ns
C_{DT}	Capacitance of C_{DT}				10	nF

SWITCHING CHARACTERISTICS (AC)

VDDI = 5 V, 0.1µF capacitor from VDDI to GNDI, VDDA = VDDB =15V, 1µF capacitor from VDDA and VDDB to GNDA and GNDB, TA = –40°C to +125°C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Switching Characteristics						
t_{PLH}	Propagation Delay, Low to High	C_{LOAD}=1nF, f_{sw}=1kHz,(50% Duty Cycle)		40	60	ns
t_{PHL}	Propagation Delay, High to Low			40	60	ns
t_r	Turn on Rise Time			6	15	ns
t_f	Turn off Fall Time			4	10	ns
t_{PWD}	Pulse Width Distortion				10	ns
t_{DM}	Propagation Delay Matching between OUTA and OUTB				10	ns
$t_{UVLO\_REC\_VDDI}$	VDDI UVLO Recovery Delay			15		µs
$t_{UVLO\_REC\_VDDA/B}$	VDDA, VDDB UVLO Recovery Delay			25	40	µs
$CMTI_H$	High Level Static Common Mode Transient Immunity	V_{CM}=1000V, T_A=25°C	100			kV/µs
$CMTI_L$	Low Level Static Common Mode Transient Immunity	V_{CM}=1000V, T_A=25°C	100			kV/µs

PARAMETER MEASUREMENT INFORMATION

Propagation Delay and Pulse Width Distortion

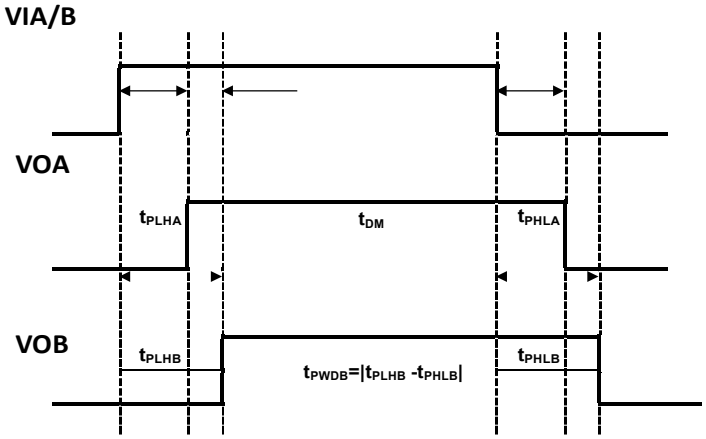


Figure 7. Propagation Delay and Pulse Width Distortion

Rise and Fall Time Testing

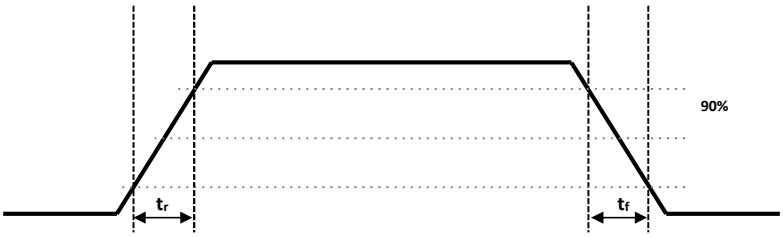


Figure 8. Turn On Rise Time and Turn Off Fall Time

CMTI Testing

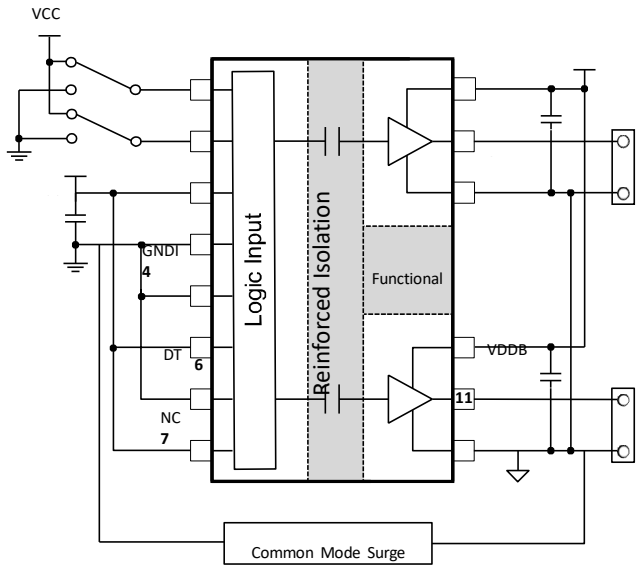


Figure 9. CMTI Test Circui

FEATURE DESCRIPTION

SGD824x is a flexible dual channel isolated gate driver that can drive IGBTs and MOSFETs. It has 4.0A peak output current capability with maxim output driver supply voltage of 25V. SGD824x has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor programmable dead time control, an DIS pin, and under voltage lock out (UVLO) for both input and output voltages.

Under Voltage Lockout

The SGD824x has under voltage lock out (UVLO) protection feature on each driver power supply voltage between the VDDA (VDDB) and GNDA (GNDB) pins. When the VDDx voltage is lower than VUVLO_VDDX_R, during device start up or lower than VUVLO_VDDX_F, after start up, the VDDA (VDDB) UVLO feature holds the driver output low, regardlessof the status of the input pins. A hysteresis on the UVLO feature prevents glitch when there is noise from the power supply.

The SGD824x also monitors the input power supply and there is an internal under voltage lock out protection featureon the VDDI. The driver outputs (VOA and VOB) are hold low when the voltage on the VDDI is lower than VUVLO_VDDI_R during start up or lower than VUVLO_VDDI_F after start up. There is a hysteresis on the VDDI UVLO featureto prevent glitch due the noise on the VDDI power supply.

Disable Input Function

When the DIS is pulled high, the VOA and VOB are pulled low regardless of the states of VIA and VIB. When the DIS pin is pulled low, the VOA and VOB are allowed for normal operation and controlled by the VIA and VIB.

The DIS input has no effect if VDDI is below its UVLO threshold and VOA, VOB remain low. There is an internal pull down resistor on the DIS pin.

Control Input and Output Logic

The VIA and VIB input controls the corresponding output channel, VOA and VOB. A logic high signal on VIA (VIB)causes the output of VOA (VOB) to go high. And a logic low on VIA (VIB) causes the output of VOA (VOB) to go low.

For PWM input versions (SGD8244), when the PWM input is high, the VOA is high and VOB is low. And when thePWM input is low, the VOA is low and VOB is high.

The Table 4 and Table 5 show the relationship between VIA,VIB, PWM, DIS, UVLO and Output of VOA and VOB.

Table 4. Relationship between Input and Output with VIA, VIB input

VIA	VIB	DIS	VDDI UVLO	VDDA UVLO	VDDB UVLO	VOA	VOB	Note
H	L	L	No	No	No	H	L	
L	H	L	No	No	No	L	H	
L	L	L	No	No	No	L	L	
H	H	L	No	No	No	H	H	Dual driver
						L	L	HS/LS
X	X	H	No	No	No	L	L	Device disabled
X	X	X	Yes	No	No	L	L	VDDI UVLO active
H	X	L	No	No	Yes	H	L	VDDB UVLO active
L	X	L	No	No	Yes	L	L	
X	H	L	No	Yes	No	L	H	VDDA UVLO active
X	L	L	No	Yes	No	L	L	

Table 5. Relationship between Input and Output with PWM input

PWM	DIS	VDDI UVLO	VDDA UVLO	VDDB UVLO	VOA	VOB	Note
H	L	No	No	No	H	L	
L	L	No	No	No	L	H	
X	H	No	No	No	L	L	Device disabled
X	X	Yes	No	No	L	L	VDDI UVLO active
H	L	No	No	Yes	H	L	VDDB UVLO active
L	L	No	No	Yes	L	L	
H	L	No	Yes	No	L	L	VDDA UVLO active
L	L	No	Yes	No	L	H	

Dead-time Program

For the high side/low side configuration driver, there is a dead-time between VOA and VOB. The dead-time delay (tDT) is programmed by a resistor (RDT) connected from the DT input to ground and it can be calculated with below equation.

$$tDT[\text{ns}] \approx 10\times RDT[\text{k}\Omega]$$

Here, tDT is the dead-time delay, RDT is the resistance value between DT and ground.

The DT pin can be connected to VDDI or left floating to provide a nominal dead time at approximately 400 ps.

A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.

The Figure 10 shows the input and output logic with dead-time in different condition.

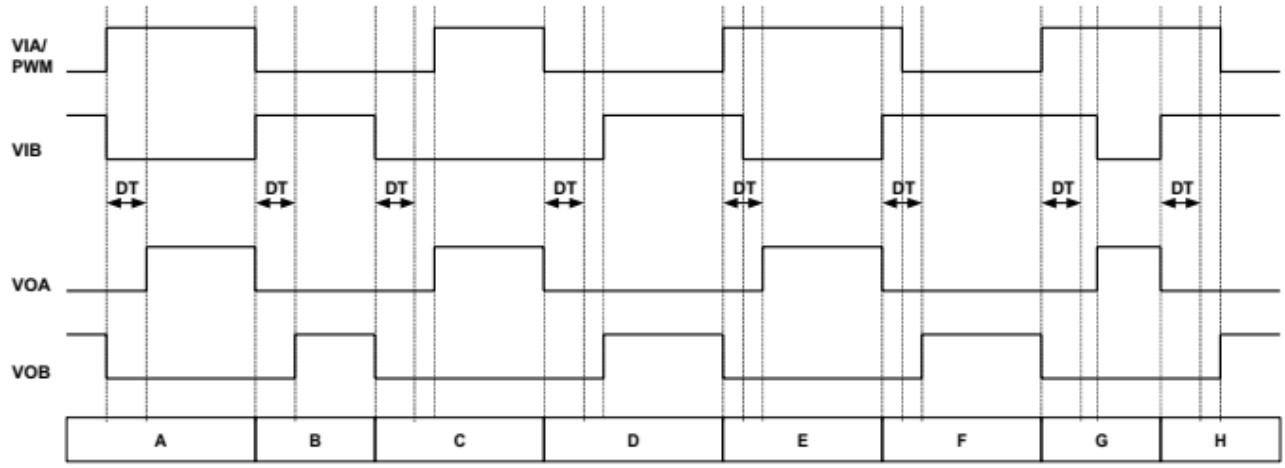


Figure 10. Input and output logic with dead-time

Condition A: VIA goes high and VIB goes low. VOB goes low immediately and VOA goes high after the programmed dead-time.

Condition B: VIA goes low and VIB goes high. VOA goes low immediately and VOB goes high after the programmed dead-time.

Condition C: VIB goes low and VIA still low. VOB goes low immediately. Since the VIA input dead-time is longer than the programmed dead-time, the VOA goes high immediately when the VIA input goes high.

Condition D: VIA goes low and VIB still low. VOA goes low immediately. Since the VIB input dead-time is

longer than the programmed dead-time, the VOB goes high immediately when the VIB input goes high.

Condition E: VIA goes high while VIB and VOB are still high, the overlap time is shorter than the programmed dead- time. To avoid overshoot, VOB goes low immediately when the VIA goes high. The VOA goes high after the programmed dead-time.

Condition F: VIB goes high while VIA and VOA are still high, the overlap time is shorter than the programmed dead- time. To avoid overshoot, VOA goes low immediately when the VIB goes high. The VOB goes high after the programmed dead-time.

Condition G: VIA goes high while VIB and VOB are still high, the overlap time is longer than the programmed dead- time. To avoid overshoot, VOB goes low immediately when the VIA goes high. Since the overlap time is longer than the programmed dead-time, the VOA goes high immediately when the VIB goes low.

Condition H: VIB goes high while VIA and VOA are still high, the overlap time is longer than the programmed dead- time. To avoid overshoot, VOA goes low immediately when the VIB goes high. Since the overlap time is longer than the programmed dead-time, the VOB goes high when the VIA goes low.

APPLICATION INFORMATION

The circuit in Figure 11 shows the typical application circuit for SGD824x to driver a typical half bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half bridge, full bridge, LLC etc. topologies and 3-phase motor drive applications.

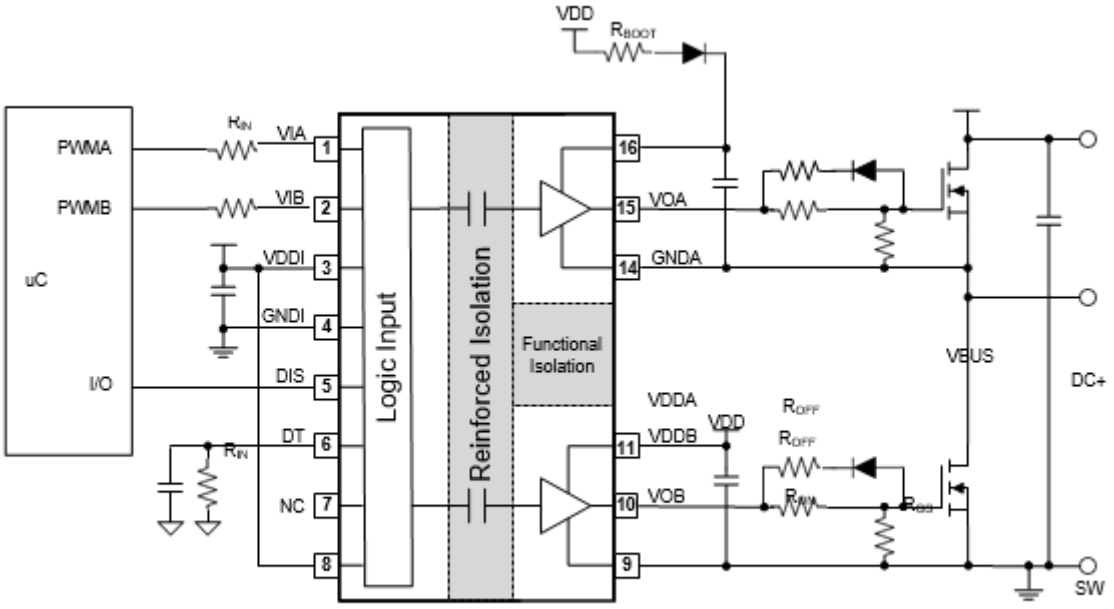
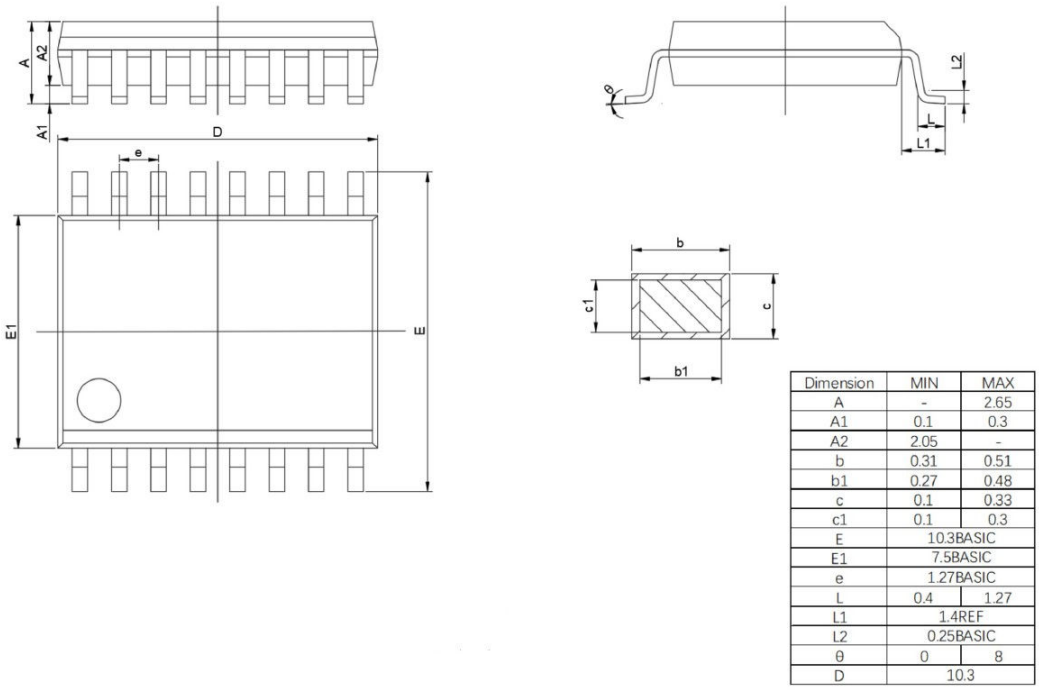


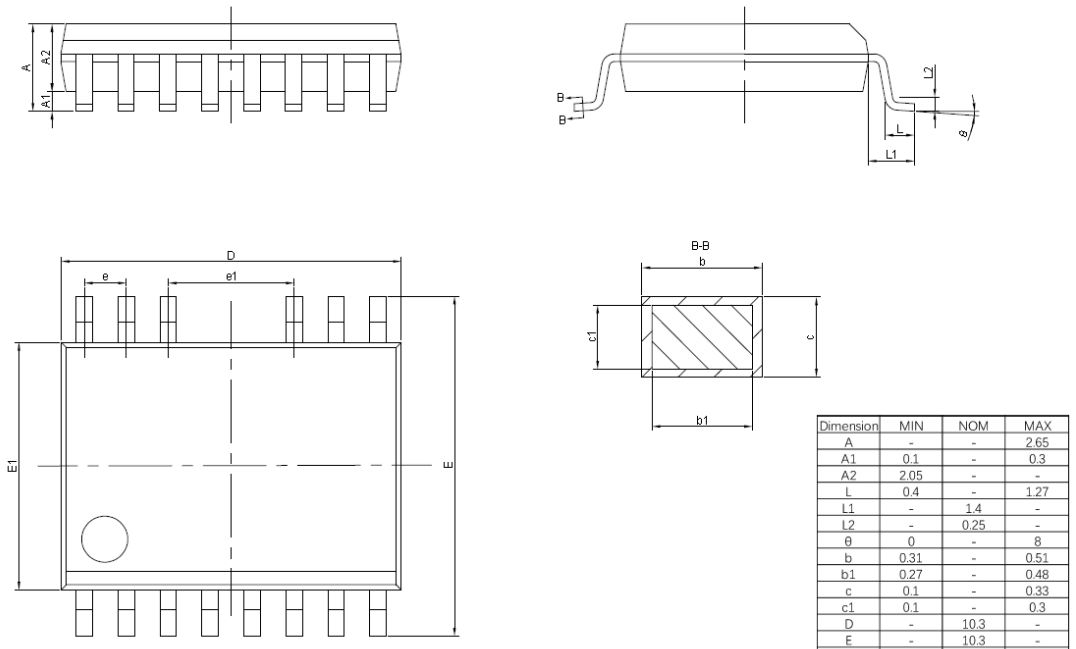
Figure 11. Typical Application Schematic

PACKAGE CASE OUTLINES



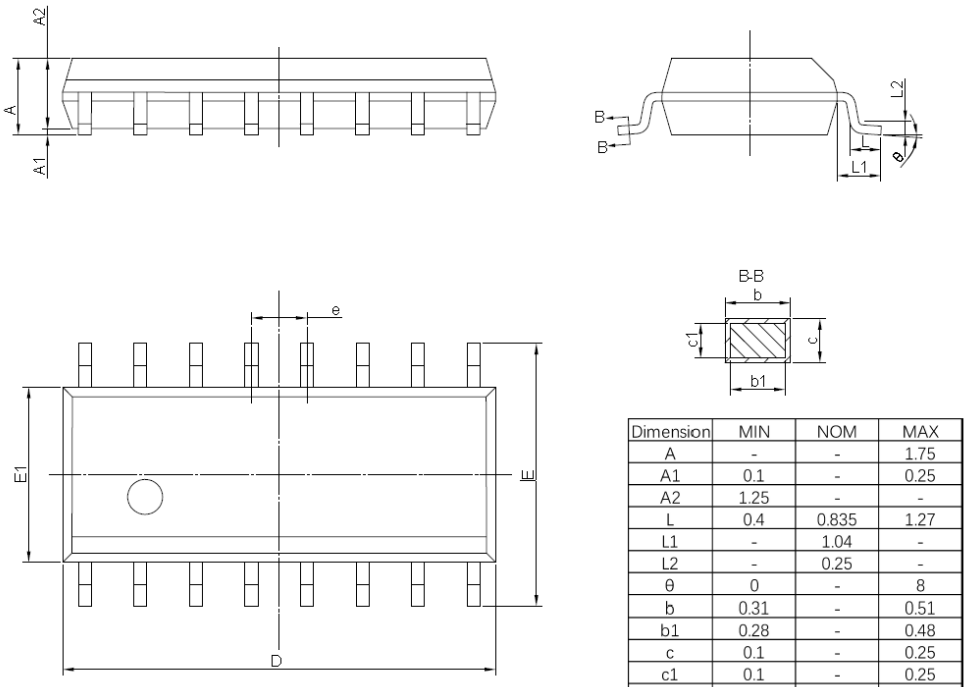
Dimension	MIN	MAX
A	-	2.65
A1	0.1	0.3
A2	2.05	-
b	0.31	0.51
b1	0.27	0.48
c	0.1	0.33
c1	0.1	0.3
E	10.3BASIC	
E1	7.5BASIC	
e	1.27BASIC	
L	0.4	1.27
L1	1.4REF	
L2	0.25BASIC	
θ	0	8
D	10.3	

Figure 12. SOP16W Package Outline Dimensions



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.05	-	-
L	0.4	-	1.27
L1	-	1.4	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.1	-	0.33
c1	0.1	-	0.3
D	-	10.3	-
E	-	10.3	-
E1	-	7.5	-
e	1.27BASIC		
e1	3.81BASIC		
Unit : mm			

Figure 13. SOP14W Package Outline Dimensions



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	-	9.9	-
E	-	6	-
E1	-	3.9	-
e	1.27 BSC		
Unit : mm			

Figure 14. SOP16 Package Outline Dimensions

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